aw_nas: A Modularized and Extensible NAS framework

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Abstract

Neural Architecture Search (NAS) has received extensive attention due to its capability to discover neural network architectures in an automated manner. aw_nas is an open-source Python framework implementing various NAS algorithms in a modularized manner. Currently, aw_nas can be used to reproduce the results of mainstream NAS algorithms of various types. Also, due to the modularized design, one can simply experiment with different NAS algorithms for various applications with aw_nas (e.g., classification, detection, text modeling, fault tolerance, adversarial robustness, hardware efficiency, and etc.). Codes and documentation are available at `https://github.com/walkerning/aw_nas`.

Keywords: neural architecture search, Python, open source

1. Introduction

Neural Architecture Search (NAS) has received extensive attention due to its capability to discover competitive neural network architectures in an automated manner. Early NAS algorithms (Zoph and Le, 2017; Real et al., 2019) are extremely slow, since a separate training phase is needed to evaluate each architecture, and tons of candidate architectures need to be evaluated to explore the large search space. Major efforts to alleviate the computational challenge of NAS lie in three aspects: 1) Better and compact search space design (Zoph et al., 2018). 2) Accelerate the evaluation of each candidate architecture (Baker et al., 2017; Elsken et al., 2018; Pham et al., 2018); 3) Improve the sample efficiency of search space exploration (Kandasamy et al., 2018; Ning et al., 2020c).

Those methods that aim to accelerate architecture evaluation can be further categorized according to whether or not the separate training phase is still needed for each architecture. Early studies shorten the separate training phase of each architecture by training curve extrapolation (Baker et al., 2017), good weight initialization (Elsken et al., 2018), and so on. On the other hand, the current trending practice, parameter-sharing evaluation, is to

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amortize architectures' training to the training of a shared set of parameters (Liu et al., 2018; Pham et al., 2018; Cai et al., 2020), thus avoid separately training each candidate architecture. From the aspect of improving the sample efficiency, a promising direction is to use predictor-based NAS methods (Kandasamy et al., 2018; Ning et al., 2020c). These methods learn a performance predictor and utilize its predictions to select architectures that are more worth evaluating.

2. aw_nas Description

aw_nas aims to provide a general, extensible and easy-to-use NAS framework, so that not only researchers can build and compare their methods in a more controlled setting, but nonprofessionals can also easily apply NAS techniques to their specific applications.

2.1 Framework Design

The main design principle lying behind aw_nas is modularization. There are multiple actors that are working together in a NAS algorithm, and they can be categorized into well-defined components based on their roles. The list of components and the aw_nas supported choices for each component are summarized in Tab. 1.

Table 1: aw_nas supported component types

Component	Description	Current supported types
Dataset	define the dataset	Cifar-10/100, SVHN, (Tiny-)ImageNet, PTB, VOC, COCO, TT100k
Objective	the rewards to learn the controller, and (optionally) the objectives to update the evaluator	classification, detection, language, fault tolerance, adversarial robustness, hardware (latency, energy ...)
Search space	define what architectural decision to be made	cell-based CNN, dense cell-based CNN, cell-based RNN, NasBench-101/201, blockwise with mnasnet/mobilenet backbones
Controller	select architectures to be evaluated	random sample, simulated annealing, evolutionary, RL-learned sampler, differentiable, predictor-based
Weights manager	fill the architectures with weights	supernet, differentiable supernet, morphism-based
Evaluator	how to evaluate an architecture	parameter-sharing evaluator (mepa), separately tune and evaluate (tune)
Trainer	the orchestration of the overall NAS search flow	a general workflow described in Sec.2.1 (simple), parallelized evaluation and async update of controller (async)

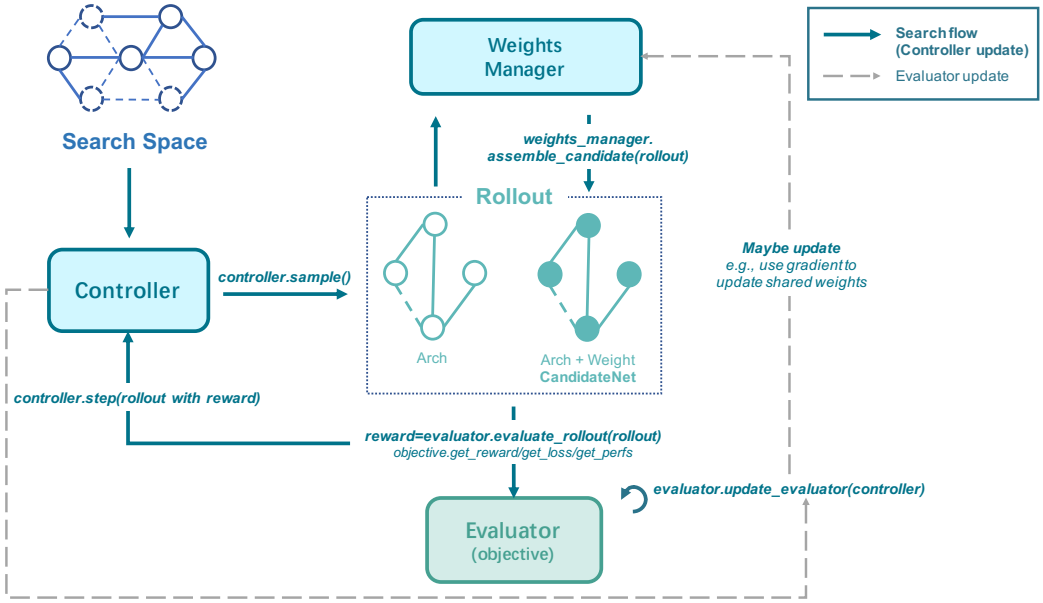

Figure 1: Search workflow and interfaces.

The interface between these components is well-defined. We use a "rollout" (class *aw-nas.rollout.base.BaseRollout*) to represent the interface object between all these components. Usually, a search space defines one or more rollout types (a subclass of *BaseRollout*). For example, the basic cell-based search space **cnn** corresponds to two rollout types: 1) **discrete** rollouts that are used in reinforcement learning (RL) based, evolutionary based controllers, and etc. 2) **differentiable** rollouts that are used in gradient-based NAS.

The search workflow of a NAS algorithm and some important interface methods are illustrated in Fig. 1. Specifically, one iteration of the search flow goes as follows:

1. *rollout = controller.sample()*: The `controller` is responsible for sampling candidate architectures from the search space.

2. *weights_manager.assemble_candidate(rollout)*: The weights manager fills the sampled architecture with weights.

3. *evaluator.evaluate_rollout(rollout)*: The evaluator evaluate the rollout that contains the architecture and weights information.

4. *controler.step(rollout)*: The rollout that contains the reward information is used to update the controller.

5. Optionally, some types of evaluator might need to be updated periodically by calling *evaluator.update_evaluator(controller)*, which might issue calls to *controller.sample* *weights_manager.assemble_candidate* too.

Taking the ENAS (Pham et al., 2018) method as an example, the `dataset` and `objective` are of type **cifar10** and **classification**, respectively. The `search space` type **cnn** defines

Table 2: aw_nas command-line utilities

Subcommand	Description
search / mpsearch	(Multiprocessing) Search for architecture
random-sample	Random sample architectures
sample	Sample architectures with a controller
derive	Derive architectures with trained NAS components
eval-arch	Eval architectures in a YAML file with an evaluator
train / mptrain / test	(Multiprocessing) Train or test an architecture
gen-(final-)sample-config	Dump the sample configuration for search (final training)
registry	Print registry information

a cell-based CNN search space. And the `controller` **rl** is a RL-learned RNN network. The `weights_manager` **supernet** is a parameter-sharing based supernet. As for the `evaluator` **mepa**, with its most basic configuration, just forward batches sampled from the dataset and call *objective.get_reward* to get the rollout's reward.

2.2 Basic Usage

aw_nas standardize a typical NAS workflow into a 3-step process, i.e., **search-derive-train**. After the search phase that is described in Sec. 2.1, the derive utility makes architecture decision using the trained NAS components. Then, a final training phase is conducted to train and evaluate the derived architecture. With aw_nas, combining various components and run a NAS algorithm is no more than just tweaking several configuration files and then run the command-line tool *awnas* with it. Currently, in aw_nas version 0.4, the available subcommands of the *awnas* command-line tool are summarized in Tab. 2.

3. Conclusion and Future Work

We introduce aw_nas, a modularized and extensible framework for NAS algorithms. By implementing various types of NAS components in a modularized way, aw_nas allows users to pick up components and run a NAS algorithm easily. An unified implementation with clear interface design also makes it easier for researchers and developers to develop and compare new NAS methods.

aw_nas is still under active development. We are trying to scale it to applications with larger scales, and make it easier for nonprofessionals to build up effective NAS systems targeted for their specific application scenarios.

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Appendix A. Some Reproducing Results and Our Researches

aw_nas can be used to reproduce many NAS algorithms by combining different components and tweaking the configurations, and some representative studies are ENAS (Pham et al., 2018), DARTS (Liu et al., 2018), SNAS (Xie et al., 2019), PC-DARTS (Xu et al., 2019), FBNet (Wu et al., 2019), OFA (Cai et al., 2020), GATES (Ning et al., 2020c), DetNAS (Chen et al., 2019), and other traditional NAS methods. We hope that, by providing a unified and modularized code base, NAS algorithms can be compared in a more controlled setting. As an example, Tab. 3 shows the reproduction results of some popular parameter-sharing NAS methods.

For more reproduction results, Fig. 2 shows the results of running OFA-based (Cai et al., 2020) search on CIFAR-10 and CIFAR-100. Due to the modularized design of aw_nas, one can easily apply a methodology to new applications. Thus, based on the OFA methodology, we utilize aw_nas to search for suitable backbones for object detection on the commonly-used VOC (Everingham et al., 2009) dataset, and show the results in Fig. 3. The algorithm flow goes as 1) Supernet training phase: Train a supernet by calling "awnas search" without controller updates, in which the sub-networks using progressive shrinking with Adaptive Distillation. 2) Search phase: Identify the Pareto front by calling "awnas search" again without evaluator updates.

Table 3: Some aw_nas reproduced results on CIFAR-10

Method	Search Time	Performance	Params (M)	FLOPs (M)
ENAS (Pham et al., 2018)	06h 17m	97.30%	4.2	1303
DARTS (Liu et al., 2018)	09h 05m	97.11%	2.59	826
SNAS (Xie et al., 2019)	08h 03m	97.02%	3.18	1029
PC-DARTS (Xu et al., 2019)	02h 57m	97.43%	4.26	1343

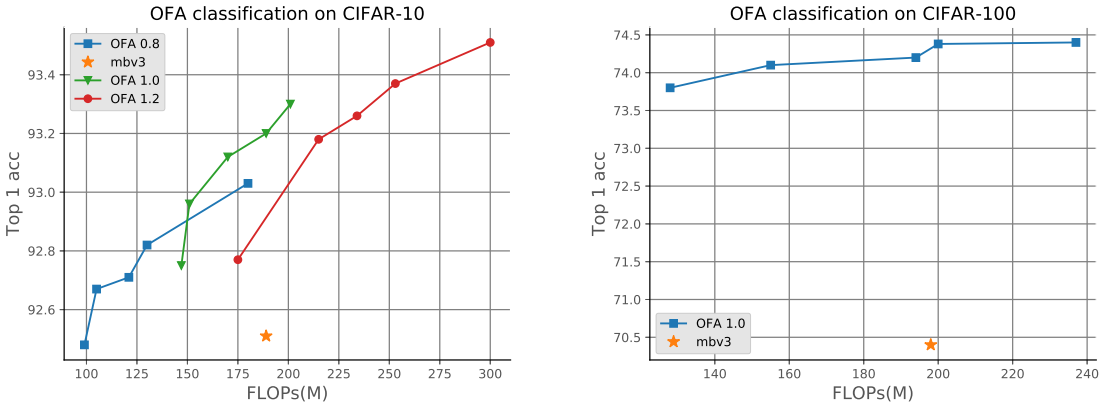


Figure 2: OFA (Cai et al., 2020) classification results on CIFAR-10 and CIFAR-100. The search space is similar to that of MobileNet-V3 (Howard et al., 2019). Sub-networks are trained using Progressive Shrinking with Knowledge Distillation and finetuned after training. 0.8, 1.0, 1.2 in the legends denote the width multiplier.

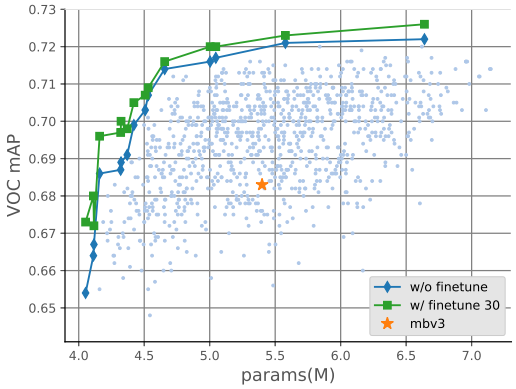


Figure 3: OFA (Cai et al., 2020) detection result on VOC. The backbone search space is similar to that of MobileNet-V3 (Howard et al., 2019), and an SSD (Liu et al., 2016) head is used. Sub-networks are trained using Progressive Shrinking with Adaptive Distillation (Tang et al., 2019) and (optionally) finetuned after training. In the search phase, 1k architectures are randomly sampled and tested (i.e., **random sample** controller is used).

Currently, our colleagues have been using aw_nas to finish various researches: 1) Applications: NAS for robust and efficient NN system at edge (Zeng et al., 2020; Li et al., 2020; Zhao et al., 2020; Ning et al., 2020b). 2) Understanding and improving NAS algorithms (Ning et al., 2020a,c).

Appendix B. Hardware Profiling Pipeline and Cost Prediction Models

Hardware-aware neural architecture search is critical for real-world tasks, especially for resource-constrained scenarios and real-time applications. aw_nas provides a set of tools and hardware cost models to support hardware-aware NAS. Namely, aw_nas has a hardware profiling toolflow that enables primitive network generation, compilation, offline profiling, and result parsing. The profiling pipeline measures the latency and energy cost of search space primitives on CPU, GPU, and FPGA platforms. From the profiled primitives' hardware cost, aw_nas can accurately estimate the candidate network's latency and energy with a set of cost prediction models. Cost prediction models and hardware cost tables for CPU, GPU, and FPGA are released as hardware assets in aw_nas.

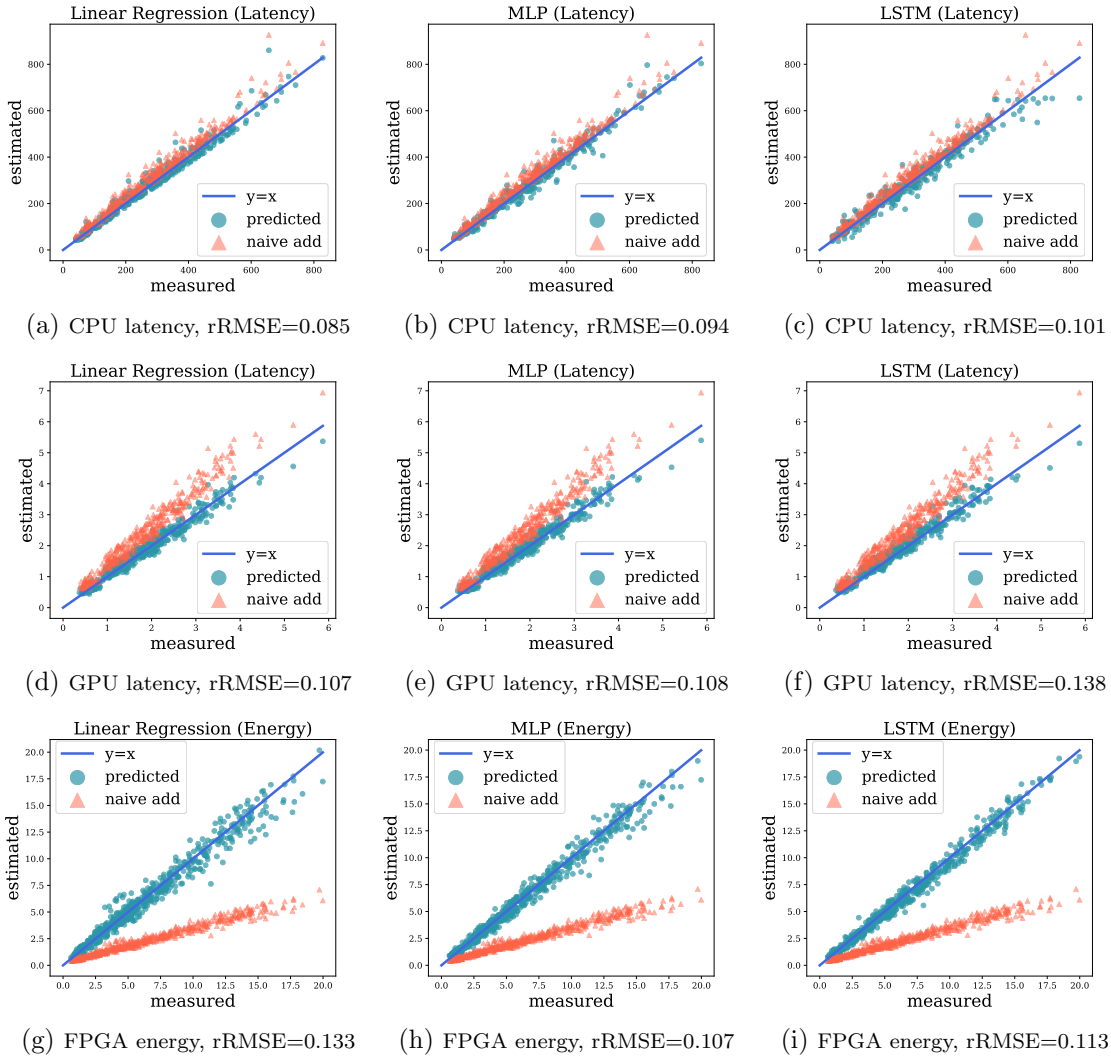
Cost prediction models are necessary because deploying all the candidate networks in NAS to a target platform is often cost-prohibitive. Moreover, the primitives' latency and energy do not always add up to the candidate network's latency and energy. On devices such as FPGA where neural networks are executed sequentially, the sum of the building blocks' latency can approximate the overall network latency to a large extent. However, on platforms with massive parallelisms, such as GPUs, the summation of block latencies can significantly deviate from the actual network latency. Energy estimation on FPGA shares the same non-linear property because the network's power does not equal the summation of its building blocks' power.

Platform	**CPU**	**GPU**	**FPGA**
Device	Intel Xeon Gold 5115	RTX-2080Ti	Xilinx ZCU102
Metrics	Latency (ms)	Latency (ms)	Latency (ms) Energy (mJ)
Profiling Tool	PyTorch	PyTorch, CuDNN	Xilinx Vitis Power Advantage Tool

Table 4: Hardware platform details for cost profiling

Three types of prediction models are currently available in aw_nas: linear regression model (1-variant or 2-variant), multilayer perceptron model (MLP), and LSTM-based model. For the single-variant linear model, the model takes the summation of primitives' latency/energy as input. For the 2-variant linear model, the input is the summation and block number. MLP model takes a vector of primitive latency as input and predicts the latency/energy for the candidate network. The structure of the LSTM model is illustrated in Fig. 5. At each time step, LSTM takes in a feature vector of block latency/energy and block configuration. More specifically, the block configuration consists of the input and output shape, kernel size, and stride. After all block features are processed, the final hidden state vector is fed into a fully-connected layer, which outputs the latency/energy prediction for the candidate network.

We conduct some experiments using aw_nas's cost prediction models for estimating CPU/GPU latency and FPGA energy in the MobileNet-V2 search space (Fig. 4). The hardware platform details are summarized in Tab. 4. We adopt the Once-For-All Cai et al. (2020) MobileNet-V2 search space design in the experiment. Specifically, a supernet with



(a) CPU latency, rRMSE=0.085 (b) CPU latency, rRMSE=0.094 (c) CPU latency, rRMSE=0.101

(d) GPU latency, rRMSE=0.107 (e) GPU latency, rRMSE=0.108 (f) GPU latency, rRMSE=0.138

(g) FPGA energy, rRMSE=0.133 (h) FPGA energy, rRMSE=0.107 (i) FPGA energy, rRMSE=0.113

Figure 4: CPU latency, GPU latency, and FPGA energy estimation using three types of prediction models (Linear regression, MLP, LSTM). For CPU latency, estimation by naively adding up block latency results in rRMSE=0.13. For GPU latency, naive addition results in rRMSE=0.253. For FPGA energy, naive addition has rRMSE=1.66. Using the prediction models, we can achieve 1.53×, 2.36×, and 15.5× better rRMSE for CPU latency, GPU latency, and FPGA energy, respectively.

five stages is constructed first (no training is needed), and candidate subnets are sampled from the supernet. Each stage in the supernet consists of numerous MobileNet-V2 inverted bottleneck blocks. When deriving candidate networks from the supernet, the number of blocks in each stage can be chosen from $\{2, 3, 4\}$ For each MobileNet-V2 block, the expansion ratio can be chosen from $\{3, 4, 6\}$, and the kernel size can be chosen from $\{3, 5, 7\}$.

Each model is trained with 2k random samples and tested on another 1k samples. Fig. 4a-4f show the prediction versus ground truth of CPU/GPU latency on test dataset,

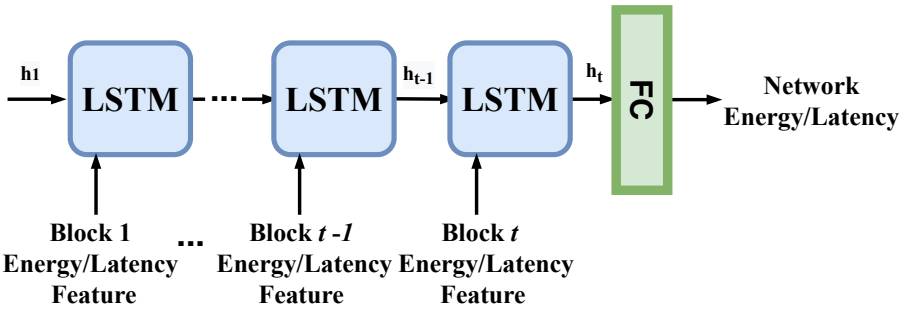


Figure 5: LSTM latency/energy hardware cost prediction model.

and Fig. 4g-4i show the prediction results for FPGA energy. Because latency/energy data of different platforms has different ranges, we measure the relative root-mean-square error (rRMSE) by:

$$rRMSE = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(\frac{Y_i - \hat{Y}_i}{Y_i})^2}$$

We observe a strong correlation between the estimated cost and the ground-truth. For CPU latency, the estimation rRMSE ranges from 0.085 to 0.101, which is up to 1.53× better than naive addition. For GPU latency, the estimation rRMSE is about 2.36× better than naive addition, ranging from 0.107 to 0.138. The latency estimation results indicate that correction models are necessary, especially for massively parallel devices such as GPUs. For FPGA energy estimation, prediction models achieve up to 15.5× improvement from naive addition.