Maximum Energy Efficiency Tracking Circuits for Converter-Less Energy Harvesting Sensor Nodes

Y. Sun, *Member, IEEE*, Zhe Yuan, Yongpan Liu, *Senior Member, IEEE*, X. Li, *Member, IEEE*, Y. Wang, Q. Wei, Yiqun Wang, *Senior Member, IEEE*, V. Narayanan, *Fellow, IEEE*, and H. Yang, *Senior Member, IEEE*

***Abstract*—Converter-less supply architecture is promising for energy harvesting sensor nodes, due to their high conversion efficiency, low cost, and easy integration. However, lack of a dc-dc converter precludes the electronic load operating under the voltage for optimal energy efficiency, since the output voltage of the energy harvester is set as the maximum power point tracking (MPPT) voltage. To mitigate efficiency loss of workload, we propose an architecture to achieve maximum energy efficiency tracking for the overall sensor node. A theoretical analysis is given for the architecture and an efficiency-driven frequency controller is fabricated to validate the design methodology. Measured results demonstrate that up to 162% performance gain of the overall sensor node is achieved compared with the existing systems with MPPT.**

***Index Terms*—Converter-less, energy efficiency, energy harvesting (EH), sensor node.**

I. Introduction

ENERGY harvesting (EH) technology has been widely investigated for ultralow power systems and self-powered sensor nodes, which can work for a couple of years. By removing the battery, EH sensor nodes achieve significant reduction of maintenance cost and environment pollution [1], [2]. Related works had existed in many aspects, such as post-CMOS devices, EH circuits, processing architectures, and high-level task scheduling [3]–[9]. Fig. 1 shows a typical architecture of an EH system with maximum power point tracking (MPPT) [10]. The EH module, such as a photovoltaic (PV) cell, harvests energy from the ambient environment, and the MPPT power converter extracts maximum power from the energy harvester. After that, the dc-dc converter generates a proper voltage for the sensor node to operate efficiently.

Manuscript received August 11, 2016; accepted October 6, 2016. Date of publication October 31, 2016; date of current version May 26, 2017. This work was supported in part by the NSFC under Grant 61674094 and Grant 61271269, in part by the Beijing Innovation Center for Future Chip and High-Tech Research and Development (863) Program under Contract 2013AA013201, in part by the NSF Awards (ASSIST) under Grant 1160483, and in part by the Center for Low Energy Systems Technology (LEAST) through by MARCO and DARPA. This brief was recommended by Associate Editor F. Lau. *(Corresponding author: Yongpan Liu.)*

Y. Sun, Z. Yuan, Y. Liu, Q. Wei, Yu Wang, and H. Yang are with the Department of Electronic Engineering, Tsinghua University, Beijing 100084, China (e-mail: ypliu@tsinghua.edu.cn).

X. Li and V. Narayanan are with the Department of Computer Science and Engineering, Pennsylvania State University, University Park, PA 16802 USA.

Yiqun Wang is with CSDDC, Wuhan 430064, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2016.2623354

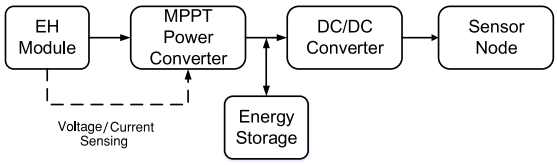


Fig. 1. Traditional architecture of EH sensor nodes.

There were plenty of works to improve the efficiency of above EH sensor nodes. A task-scheduling algorithm is proposed [11] to regulate tasks at the lowest possible speed for better energy efficiency. Furthermore, a power-management mechanism that is compliant with indoor irradiance is introduced [12]. Later, a system on chip (SoC) is fabricated [13], in which a multioutput energy efficient dc-dc converter is adopted. However, most of previous systems suffer from the energy loss of power converters. Even worse, the area and cost overheads of dc-dc converters become critical bottleneck for emerging applications, such as implanted devices.

Recently, converter-less sensor nodes raise more and more attentions. A fully integrated power-management system for micro-power solar EH applications is implemented [14]. Furthermore, a converter-less and storage-less EH system with MPPT is proposed [15], which improves the energy efficiency by 20%. However, the removal of dc-dc converters sacrifices the voltage adaption of sensor nodes. Even if the output voltage of energy harvester is set as the MPPT value to collect the maximum energy, the energy efficiency of the workload may be poor under the optimal MPPT voltage.

As shown in Fig. 2, the solid curve indicates the energy efficiency of electronic load under different operating voltages. When the voltage goes down, the circuits become slow but their energy efficiency increases. The energy efficiency reaches a peak when the supply voltage locates in the near-threshold range of the transistors [16]. Obviously, the MPPT voltage for the energy harvester is inconsistent with the optimal supply voltage of electronic load. From the system-level point of view, the overall energy efficiency is determined by the product of that of the energy harvester and the electronic load, implying a tradeoff to be made.

Inspired by the observation, an EH architecture is proposed to support optimal energy efficiency tracking by voltage

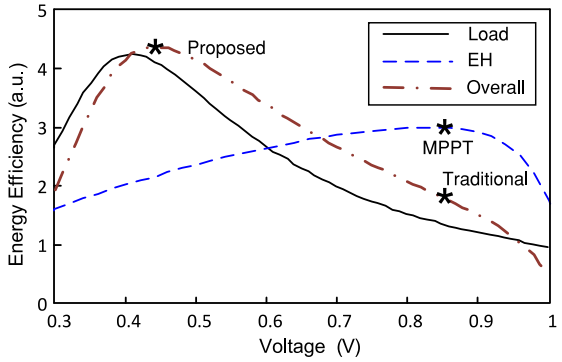


Fig. 2. Energy efficient as a function of supply voltage.

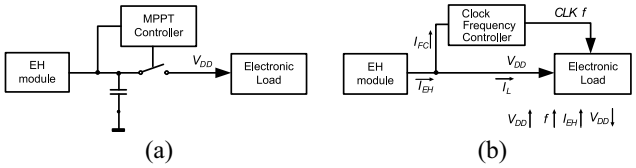


Fig. 3. (a) Converter-less MPPT architecture [15]. (b) Proposed architecture.

adaption. Different from MPPT, it optimizes the overall energy efficiency of sensor nodes, instead of the energy harvester only. Section II proposes the theoretical analysis of energy efficiency for the converter-less EH architecture and the optimal conditions to achieve the best overall energy efficiency, based on which efficiency-driven frequency controller circuits are designed in Section III. A proof-of-concept circuit is silicon fabricated to prove the methodology and measured results demonstrate 162% improvement over the state-of-the-art method in Section IV.

II. System Architecture

In this section, we first show the proposed architecture and its advantages compared with existing systems. After that, we define the system-level energy efficiency for the converter-less architecture and prove a theorem about the optimal efficiency. Finally, a case study is provided to guide the design exploration of the control circuit.

A. Architecture Overview

Previous converter-less EH works [15] maximize the energy efficiency of the harvester. However, the system-level energy efficiency may not reach the highest level due to the lack of dc-dc converters, which makes the supply voltage of the workload stay at a suboptimal level. In order to make the system work at the supply voltage with the highest energy efficiency, an adaptive voltage-controlled clock frequency controller (CFC) is proposed. As shown in Fig. 3(b), the proposed architecture has three main parts: 1) EH; 2) CFC; and 3) electronic workload (EL). The electronic load is composed of digital processors, analog and radio-frequency circuits. The supply voltage of the digital processor can be tuned in a range, while the analog and radio-frequency circuits can be switched off and on. In typical sensing cases, the digital processor and ultralow power sensors of electronic load are activated for power savings.

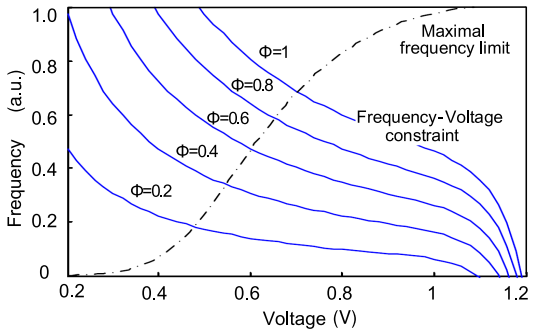


Fig. 4. Frequency-voltage constraints and feasible operation of workload.

Different from the conventional power track architecture shown in Fig. 1, the supply voltage of the workload is automatically adjusted by the feedback loop of EH, CFC, and EL shown in Fig. 3. When more energy is harvested, the supply voltage V_{DD} rises $\uparrow$ and the output frequency of CFC f increases $\uparrow$, which makes the EL running faster and drawing more current I_{EH} $\uparrow$ from the EH. It will lower the supply voltage V_{DD} $\downarrow$ in the opposite direction. When a proper supply voltage is reached, the equilibrium of the system can be achieved and vice versa.

The CFC can generate the optimal supply voltage and clock frequency to EL through the feedback loop. The adaptive capability avoids two disadvantages in traditional converter-less systems.

1) When the gathered energy is insufficient, the supply voltage will drop below the critical voltage in previous system and lead to power failures.
2) When the incoming energy is larger than the present energy consumption of EL, there will be energy overflow and thus energy wastes if the system can not rise the operating frequency of EL.

B. Theoretical Analysis

Before designing the CFC circuit, we first define the optimal energy efficiency metric. $E_{\mathrm{Env}} = \int_{t_0}^{t_1} \phi(t)dt$ denotes the input energy to the harvester in a period $[t_0, t_1]$, where $\phi(t)$ is the environment power fed into the harvester. E_{EH} represents the output energy generated by the harvester. E_{EL} is the energy consumption of the EL. The work effort is characterized by the completed clock cycles ($\#\mathrm{Op} = \int_{t_0}^{t_1} f(t)dt$) by the digital circuit in the same period $[t_0, t_1]$, where $f(t)$ is the clock frequency of the digital circuit. The system-level energy efficiency η is defined as

$$\eta = \frac{\#\mathrm{Op}}{E_{\mathrm{Env}}} = \frac{E_{\mathrm{EH}}}{E_{\mathrm{Env}}} * \frac{E_{\mathrm{EL}}}{E_{\mathrm{EH}}} * \frac{\#\mathrm{Op}}{E_{\mathrm{EL}}}. \quad (1)$$

The overall energy efficiency is the product of three parts: The first part is the energy efficiency of EH; the second one is approximately equal to one in the converter-less architecture. The last one is the energy efficiency of EL. The CFC can balance these factors to achieve the optimal η.

As there is no energy buffer, the clock frequency $f(t)$ of the EL at time t is limited by two factors: 1) the fastest frequency that the EL can run and 2) the maximal current that the EH can provide. Given a digital circuit, its maximal operating frequency can be adjusted in a range by tuning the supply voltage (V_{DD})

$$f \le h(V_{\mathrm{DD}}). \tag{2}$$

Fig. 4 shows the maximal operating frequency of the EL under different supply voltages by the dotted line.

The other constraint on the current balance is illustrated as follows. The supply voltage V_{DD} of an EH is determined by the environment power ϕ (e.g., solar irradiance power for PV cells) and the output current I_{EH}

$$V_{\mathrm{DD}} = V_{\mathrm{EH}}(\phi, I_{\mathrm{EH}}). \tag{3}$$

Based on the Kirchhoff's circuit laws, we have

$$I_{\mathrm{EH}}(\phi, V_{\mathrm{DD}}) = I_L(f, V_{\mathrm{DD}}) + I_{\mathrm{FC}}(V_{\mathrm{DD}}) \tag{4}$$

where the current of the EL I_L is determined by the supply voltage V_{DD}, the clock frequency f, and the current of the CFC I_{FC} (refer to the Appendix for details). Base on (3) and (4), we have the constraint between the clock frequency f of the EL and the supply voltage V_{DD} under different solar irradiance ϕ

$$f = g(V_{\mathrm{DD}}, \phi) \tag{5}$$

shown by the solid curves in Fig. 4. The lemma in the Appendix proves that those curves are monotonically decreasing, which implies that a higher frequency f of the EL will lead to a lower supply voltage V_{DD}.

It is intuitively to conclude that the maximal energy efficiency of overall system can be achieved when the system works at the interaction points by the solid and dotted curves in Fig. 4. A theorem is proposed as below.

Theorem: The optimal $\eta_{\max}$ can be reached in the converterless architecture, when the EL can satisfy both its maximal clock frequency constraint $h(V_{\mathrm{DD}})$ and the frequency-voltage constraint of the EH

$$\eta = \eta_{\max} \quad \text{when } f = h(V_{\mathrm{DD}}) = g(V_{\mathrm{DD}}, \phi).$$

Proof: The peak operating frequency of EL $h(V_{\mathrm{DD}})$ increases monotonously with the supply voltage V_{DD}

$$\mathrm{d}h(V_{\mathrm{DD}})/\mathrm{d}V_{\mathrm{DD}} > 0. \tag{6}$$

However, the operating frequency f of EL should be less than $h(V_{\mathrm{DD}})$ to avoid timing violation

$$f \le h(V_{\mathrm{DD}}). \tag{7}$$

A lemma in the Appendix proved that the higher clock frequency the EL operates at, the lower supply voltage the EH module can supply

$$\mathrm{d}f/\mathrm{d}V_{\mathrm{DD}} = \mathrm{d}g(V_{\mathrm{DD}}, \phi)/\mathrm{d}V_{\mathrm{DD}} < 0. \tag{8}$$

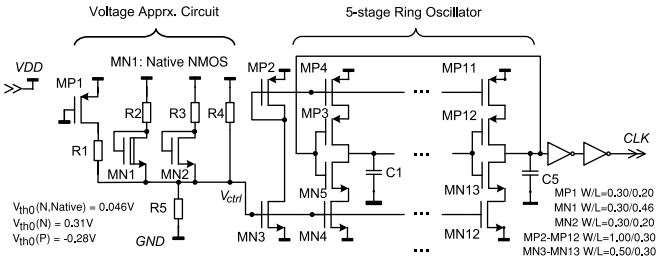


Fig. 5. Resistor-based CFC diagram.

Thus, there exists one and only one V_{DD} to satisfy

$$f = h(V_{\mathrm{DD}}) = g(V_{\mathrm{DD}}, \phi). \tag{9}$$

When the supply voltage of EL is V_{DD}, the clock frequency of EL should satisfy both $h(V_{\mathrm{DD}})$ and $g(V_{\mathrm{DD}}, \phi)$ to achieve the optimal energy efficiency. Theorem is proved. ■

The theorem illustrates that the optimal supply voltage and frequency of the EL is dynamically determined by the environment input power ϕ. As shown in Fig. 3(b), the CFC is used to track and generate the optimal clock frequency of the EL. According to theorem, it should approximate the intersection points of $h(V_{\mathrm{DD}}) = g(V_{\mathrm{DD}}, \phi)$ to achieve $\eta_{\max}$.

III. CFC Circuit Analysis and Implementation

This section shows the circuit design of CFC to achieve the optimal system-level energy efficiency. After that, a parameter optimizing methodology is provided.

A. Resistor-Based CFC Implementation

To illustrate the effectiveness of the proposed methodology, we propose a resistor-based CFC implementation, which is a proof-of-concept of the proposed architecture. More advanced structures can provide better performance at the cost of area overheads and design efforts. However, Section IV demonstrates that the resistor-based implementation has a rather good approximation.

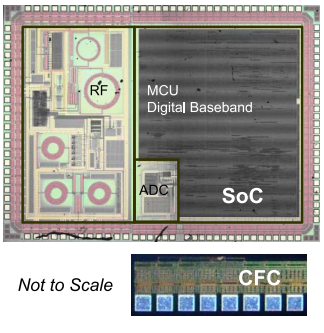
As shown in Fig. 5, the controller consists of a five-stage voltage-controlled ring oscillator to generate the optimal frequency and a control circuit is used to generate the control voltage V_{ctrl} for the oscillator. The control circuit is composed by resistors and transistors with different threshold voltages to generate a nonlinear relationship between V_{ctrl} and V_{DD}. The function between the output frequency f and V_{DD} is decided by the values of resistors R_i, $i = 1, \ldots, 5$

$$f = f_{R_i}(V_{\mathrm{DD}}). \tag{10}$$

As (10) has shown, different configurations of R_i, $i = 1, \ldots, 5$, result in a different frequency-voltage constraint of the EL.

B. Parameter Optimizing Methodology

Given the environment input power $\phi(t)$, $f_{R_i}(\phi)$ is generated by CFC configured by the resistor value R_i. Since the optimal frequency with the highest overall efficiency is



Clock Frequency Controller (CFC)	
Process	0.13um
Size	45um*22um (w/o pads)
SoC (Load)	
Process	0.13um
Size	3.4mm*2.5mm
Voltage (Digital Part)	0.35-1.2V
Power (Digital Part)	30uW-1.23mW
Solar Cell (2 series)	
Total Size	15mm^2
Open Voltage (1000W/m^2)	1.1V
Short Current (1000W/m^2)	1.6mA

Fig. 6. Die photos of the SoC workload and CFC.

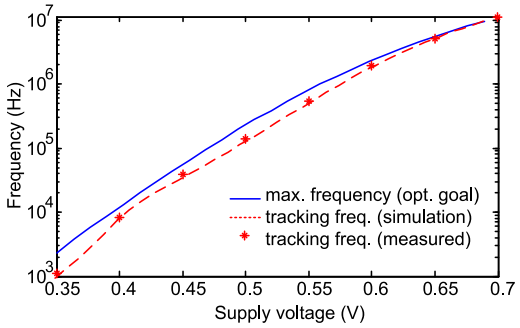


Fig. 7. Tracking the maximum frequency of the electronic load.

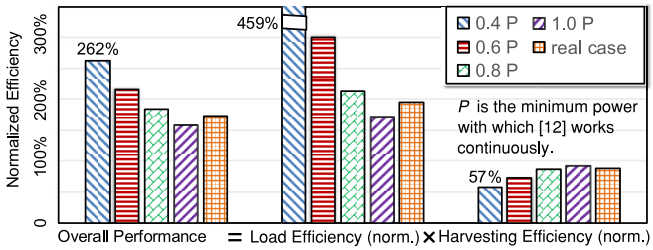


Fig. 8. Efficiency improvement compared with [15].

$f(\phi)$ specified by theorem, the parameter optimization is to minimize the difference between $f(\phi)$ and $f_{R_i}(\phi)$ by selecting proper values of resistors. Furthermore, the optimization should be weighted by the occurrence probability of different power levels. Assuming that the cyclostationary process $\phi(t)$ in $[t_0, t_1]$ follows a distribution pdf(ϕ), the optimization problem is formulated as

$$\text{obj.: } \min \int_0^{\infty} \big(f(\phi) - f_{R_i}(\phi)\big)\text{pdf}(\phi)\text{d}\phi \tag{11}$$

$$\text{s.t.: } f(\phi) - f_{R_i}(\phi) > 0. \tag{12}$$

The constraint (12) is used to avoid timing violations, as the operating frequency under any environment power input should be smaller than the maximal frequency of the EL. This optimization can be solved by sequential quadratic programming. We implement a solver in MATLAB to determine values of resistors. The source code and circuit netlist are available via e-mail.

IV. Experimental Results

A. Experimental Setup

The prototype consists of a low-power SoC for wireless body area network [17] and the proposed frequency controller (CFC). Both chips are fabricated in 0.13 μm technology and their configurations and die photos are shown in Fig. 6. The active area of CFC is less than 0.001 mm^2, which is negligible compared with the SoC. We adopt two serial connected 15 mm^2 equivalent size PV cells to power the SoC. The environment power inputs are extracted from the measured solar irradiance data [18] for the optimization method in Section III. The power consumption is measured by a data acquisition board.

B. Energy Aware Frequency Tracking

The optimal frequency tracking curve can be extracted from the simulations or measurement results of SoC. In Fig. 7, the solid blue line represents the optimal frequency under different power inputs, which lead to different supply voltages. Based on (12), we can design a CFC circuit to track the curve by tuning the resistance values. The red dotted line shows the frequency tracking results with the proposed CFC by simulations, where $R_1 = 32$ kΩ, $R_4 = 297$ kΩ, and $R_5 = 150$ kΩ, and both R_2 and R_3 are open (∞). The size of transistors in CFC is also provided in Fig. 5.

The measured results of the CFC chip are plotted as star points, which are well matched with the target red dotted points. We can conclude that the proposed design methodology and CFC circuits can approximate the optimal frequency-voltage curve well. The next section shows that CFC can achieve significant performance improvements with trivial area overhead, which implies that the design realizes a proper tradeoff between area overhead and performance. More complex tracking circuits may achieve better results but at the cost of larger area.

C. Energy Efficiency Comparison

We demonstrate that the energy efficiency of overall system [defined in (1)] can be maximized under the proposed CFC compared with the traditional MPPT circuit in a converter-less EH sensor node. The converter-less architecture [15] is used as the baseline. The energy efficiency of the proposed CFC-based sensor node is normalized to the baseline. Several different power traces are used as the inputs to measure the effectiveness of the proposed architecture under different cases. No timing errors or control loop instability is observed in the experiments.

Fig. 8 compares the normalized efficiency of the overall sensor node, the EH and the EL under different ambient energy levels. The overall energy efficiency can be improved by 162%. The improvement comes from the energy efficiency tradeoff between workload and energy harvester. In the MPPT approach, it maximizes the efficiency of the EH, while the efficiency of the EL is quite low. The proposed approach makes a better tradeoff and automatically chooses the best voltage and frequency to achieve the optimal energy efficiency.

Furthermore, it is shown that the proposed method is more effective when the ambient power level is low. It is because that the optimal supply voltage will be low when the input power level is low, but the energy efficiency of the EL is much higher under the low supply voltage.

V. Conclusion

This brief presents an architecture without energy storage elements or dc/dc converters for low power EH systems. Different from traditional converter-less work, we consider the overall system energy efficiency instead of that of the EH only. We prove a theorem to show the optimal frequency-voltage curve to achieve overall system energy efficiency under different ambient power inputs, based on which a CFC circuit is proposed to validate its effectiveness. A prototype is fabricated to test the proposed architecture. Up to 162% performance gain is observed compared with the existing storage-less and converter-less work. Our future work is to integrate the architecture into SoC and adopt low voltage nonvolatile memory for transient powered devices.

Appendix

Proof of the Lemma

In the proposed architecture, the higher clock frequency f the workload operates, the lower voltage ($V_{\rm DD}$) the EH module can supply at any fixed environment input power

$$\mathrm{d}f/\mathrm{d}V_{\rm DD} < 0.$$

Proof: Without losing generality, we will prove this lemma holds for PV cells. Similarly, it also holds for other energy harvesters. The output current $I_{\rm EH}$ of PV cells can be modeled as

$$I_{\rm EH} = I_P(\phi) - I_0\left(e^{\frac{V_{\rm DD}+R_sI_{\rm EH}}{nV_T}} - 1\right) - \frac{V_{\rm DD}+R_sI_{\rm EH}}{R_p} \tag{13}$$

where n, I_0, ϕ, $V_T = kT/q, R_s, R_p$ indicate the number of PV cells, current coefficient of diode, solar irradiance, thermal voltage, equivalent series, and parallel resistors, respectively. In (4), the current of the digital circuit load includes dynamic part and leakage part

$$I_L(f, V_{\rm DD}) = I_{\rm dyn} + I_{\rm lkg}(V_{\rm DD}) \tag{14}$$

$$\approx \alpha C V_{\rm DD} f + I_{\rm lkg}(V_{\rm DD}) \tag{15}$$

where α is average switching activity, and C is the equivalent capacitor of the circuit. According to (4), we have

$$\frac{\partial I_{\rm EH}}{\partial V_{\rm DD}}\mathrm{d}V_{\rm DD} = \frac{\partial I_L}{\partial f}\mathrm{d}f + \frac{\partial I_L}{\partial V_{\rm DD}}\mathrm{d}V_{\rm DD} + \frac{\partial I_{\rm FC}}{\partial f}\mathrm{d}f + \frac{\partial I_{\rm FC}}{\partial V_{\rm DD}}\mathrm{d}V_{\rm DD}. \tag{16}$$

That is

$$\frac{\mathrm{d}f}{\mathrm{d}V_{\rm DD}} = \frac{\frac{\partial I_{\rm EH}}{\partial V_{\rm DD}} - \frac{\partial I_L}{\partial V_{\rm DD}} - \frac{\partial I_{\rm FC}}{\partial V_{\rm DD}}}{\frac{\partial I_L}{\partial f} + \frac{\partial I_{\rm FC}}{\partial f}}. \tag{17}$$

Note $I_{\rm EH}$ is a function of φ and $V_{\rm DD}$, while I_L and $I_{\rm FC}$ are functions of f and $V_{\rm DD}$. According to (13) and (14), we have

$$\partial I_{\rm EH}(\phi, V_{\rm DD})/\partial V_{\rm DD} < 0 \tag{18}$$

$$\frac{\partial I_L}{\partial V_{\rm DD}} = \alpha C f + \frac{\partial I_{lkg}(V_{\rm DD})}{\partial V_{\rm DD}} > 0 \tag{19}$$

$$\frac{\partial I_L}{\partial f} = \alpha C V_{\rm DD} > 0 \tag{20}$$

$$\frac{\partial I_{\rm FC}}{\partial V_{\rm DD}} > 0, \quad \frac{\partial I_{\rm FC}}{\partial f} > 0. \tag{21}$$

Hence, we have

$$\mathrm{d}f/\mathrm{d}V_{\rm DD} < 0. \tag{22}$$

■

References

[1] Y.-J. Kim, H. S. Bhamra, J. Joseph, and P. P. Irazoqui, "An ultra-low-power RF energy-harvesting transceiver for multiple-node sensor application," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 11, pp. 1028–1032, Nov. 2015.

[2] W. Xu, X. Li, W. Li, H. Yuan, and G. Wang, "Live demonstration: An optimization software and a design case of a novel dual band wireless power and data transmission system," in *Proc. IEEE ISCAS*, Melbourne, VIC, Australia, 2014, p. 436.

[3] Y. Liu *et al.*, "Ambient energy harvesting nonvolatile processors: From circuit to system," in *Proc. IEEE DAC*, San Francisco, CA, USA, 2015, pp. 1–6.

[4] Y. Liu *et al.*, "4.7 A 65nm ReRAM-enabled nonvolatile processor with 6× reduction in restore time and 4× higher clock frequency using adaptive data retention and self-write-termination nonvolatile logic," in *Proc. IEEE ISSCC*, San Francisco, CA, USA, 2016, pp. 84–86.

[5] Y. Wang *et al.*, "A 3us wake-up time nonvolatile processor based on ferroelectric flip-flops," in *Proc. IEEE ESSCIRC*, Bordeaux, France, 2012, pp. 149–152.

[6] Y. Wang *et al.*, "PaCC: A parallel compare and compress codec for area reduction in nonvolatile processors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 7, pp. 1491–1505, Jul. 2014.

[7] L. Liu, J. Xu, N. Ma, and Z. Zhu, "A hybrid threshold self-compensation rectifier for RF energy harvesting," *IEICE Electron. Exp.*, vol. 11, no. 23, pp. 1–7, Nov. 2014.

[8] K. Ma *et al.*, "Architecture exploration for ambient energy harvesting nonvolatile processors," in *Proc. IEEE HPCA*, Burlingame, CA, USA, 2015, pp. 526–537.

[9] D. Zhang *et al.*, "Solar power prediction assisted intra-task scheduling for nonvolatile sensor nodes," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 35, no. 5, pp. 724–737, May 2016.

[10] T. Esram and P. L. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 439–449, Jun. 2007.

[11] S. Liu, J. Lu, Q. Wu, and Q. Qiu, "Harvesting-aware power management for real-time systems with renewable energy," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 8, pp. 1473–1486, Aug. 2012.

[12] B. Tar and U. Çilingiroğlu, "Nanowatt-scale power management for on-chip photovoltaic energy harvesting beacons," *IEEE J. Emerg. Sel. Topic Circuits Syst.*, vol. 4, no. 3, pp. 284–291, Sep. 2014.

[13] A. Klinefelter *et al.*, "A 6.45μW self-powered IoT SoC with integrated energy-harvesting power management and ULP asymmetric radios," in *Proc. IEEE ISSCC*, San Francisco, CA, USA, 2015, pp. 384–385.

[14] N. Khosropour, F. Krummenacher, and M. Kayal, "Fully integrated ultra-low power management system for micro-power solar energy harvesting applications," *Electron. Lett.*, vol. 48, no. 6, pp. 338–339, Mar. 2012.

[15] C. Wang *et al.*, "Storage-less and converter-less maximum power point tracking of photovoltaic cells for a nonvolatile microprocessor," in *Proc. IEEE ASP-DAC*, Singapore, 2014, pp. 379–384.

[16] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," *Proc. IEEE*, vol. 98, no. 2, pp. 253–266, Feb. 2010.

[17] B. Zhao *et al.*, "An energy efficient fully integrated OOK transceiver SoC for wireless body area networks," in *Proc. IEEE A-SSCC*, Singapore, 2013, pp. 441–444.

[18] S. Wilcox, "National solar radiation database 1991–2010 update: User's manual," U.S. Dept. Energy, Nat. Renew. Energy Lab., Golden, CO, USA, Tech. Rep. NREL/TP-5500-54824, 2012.