Abstract—Recent advances in memristor technology lead to the feasibility of large-scale neuromorphic systems by leveraging the similarity between memristor devices and synapses. For instance, memristor cross-point arrays can realize dense synapse network among hundreds of neuron circuits, which is not affordable for traditional implementations. However, little progress was made in synapse designs that support both static and dynamic synaptic properties. In addition, many neuron circuits require signals in specific pulse shape, limiting the scale of system implementation. Last but not least, a bottom-up study starting from realistic memristor devices is still missing in the current research of memristor-based neuromorphic systems. Here, we propose a memristor-based dynamic (MD) synapse design with experiment-calibrated memristor models. The structure obtains both static and dynamic synaptic properties by using one memristor for weight storage and the other as a selector. We overcame the device nonlinearities and demonstrated spike-timing-based recall, weight tunability, and spike-timing-based learning functions on MD synapse. Furthermore, a temporal pattern learning application was investigated to evaluate the use of MD synapses in spiking neural networks, under both spike-timing-dependent plasticity and remote supervised method learning rules.

Index Terms—Memristor, neural network hardware, synapse.

I. INTRODUCTION

SPIKING neural networks (SNNs) increases the level of realism in neural simulations by incorporating time into neuron/synapse models [1]. Since information is encoded by the precise timing of spikes, a train of spikes can contain more information than binary/rate encoding methods. Moreover, SNNs minimize the data communication cost by distributing data into local memories (i.e., synapses) close to the associated computing units (i.e., neurons) throughout the entire system. SNNs can reduce the communication cost and consequently may achieve brain-level computing efficiency [2]. For example, TrueNorth—the latest spike-timing-based neuromorphic hardware prototyped by IBM achieved an extremely low energy consumption of 45 pJ per spike for data communication [3]. However, conventional CMOS implementation of synapse design suffers from large area, high power consumption, and low-level parallelism. In TrueNorth, one digital neuron circuit is multiplexed to model 256 neurons, and a 256 kBit SRAM is used for neuron data storage. Another SRAM for synapse weight works in parallel to update the neuron information, each synapse weight can only be chosen from one of −2, −1, 0, 1, and 2. As a result, the speed, size and bit-accuracy of neural network are limited by the SRAM: not only the sequential update of SRAM for neuron data storage limits the final system speed, but also the SRAM for synapse weight has very limited bit-accuracy and both together take a major part of the chip area. Last but not least, the majority of system energy was also consumed on SRAM reading/writing in recall and learning operations [2], [4].

Memristor technology has gained significant attention in the neuromorphic system community since the first physical device demonstration in 2008 [5]. Electrical measurements demonstrated that memristors can produce many important features of biological synapses, such as long-term potentiation (LTP), long-term depression (LTD), spike-timing-dependent plasticity (STDP), and short-term potentiation (STP) [6]–[15]. More importantly, the two-terminal structure of memristors enables the cross-point array implementation with high storage density and sub-pJ access energy [16]. Fully parallel recall operations through a cross-point array which applies synaptic weights to input signals and sends their summation to output neurons have been demonstrated in the latest research [17]. Last but not least, comparing to state of the art digital implementations, memristor-crossbar-based system shows orders of magnitude better energy efficiency and speed in both inferencing [18] and training neural network algorithms [19].

Various neuromorphic circuits using single memristors to construct synapses have been presented [6]–[9]. However, these approaches are still far from mimicking synaptic models in SNNs. For example, the popular α-function synaptic model [20] transforms an input voltage spike from preneuron to an α-function shaped current signal and passes it to post-neuron. The transformed current signal is a function of
the input spiking time and the spatial weight of the synapse. Biological synapses exhibit even richer dynamic behaviors corresponding to more complex models [21], [22]. In other words, a synapse cannot be simply taken as a static resistor but reveals dynamic property.

A common way of realizing both static and dynamic properties at software level is to integrate a dynamic synapse model into a spike-timing-based learning algorithm [1], [20], [23]. Currently, most of memristor-based synapse designs are based on multilevel/analog memristor value. Once learning is completed, the synaptic weight remains constant while the corresponding transformation function is performed in neuron circuit, through pulse shape modulator. As illustrated in Fig. 1, instead of spikes, a neuron circuit generates transformed signals to synapses [6]–[9]. Although many single-memristor based synapse designs demonstrated STDP feature theoretically and experimentally, the approach is not feasible for large-scale neural network implementation for the following reasons.

1) The neuron design complexity increases dramatically with the number of synapses, which is well known as fanout issue.
2) It is difficult to preserve the quality of transformed signals that degrade rapidly as synapse number increases.

To enable the use of memristor-based synapse in large-scale neural network implementation, we propose a novel design named as memristor-based dynamic (MD) synapse that provides the following features.

1) In-situ dynamic transformation function determined by both static weight and relative dynamic spiking timing at pre- and post-neurons.
2) Two-terminal structure that can be easily integrated in a cross-point array for massive connections.
3) Relaxation in spike signal requirement which helps reduce neuron design complexity and improve communication energy efficiency.
4) Support of typical synaptic properties, including spike-timing-based recall and synaptic weight tuning.
5) Spiking-timing based learning demonstrated by utilizing fundamental STDP [23] and remote supervised method (ReSuMe) [20] learning rules.

Furthermore, we studied the use of MD synapses in SNNs by taking a temporal pattern learning task as example. Our results showed that the learning task can be accomplished at the nano-second scale with average 36.7 and 64.0 pJ per learning spike for STDP and ReSuMe learning rules, respectively. The recall energy consumption is only 14.6 pJ per recall spike without including the energy consumed by pre- and post-neurons. All the simulations were performed with the experimentally calibrated TaOx memristor model [24], providing a strong device foundation for the results.

This paper is organized as follows. Section II gives a brief introduction on synapse and SNNs. Section III describes the proposed MD synapse design and analyzes its electrical characteristics. Section IV validates the synaptic properties of the MD synapse design. Section V demonstrates its applications in an SNN for a learning task and studies the design efficacy. Extended discussions regarding about the circuit implementation and the selection of memristor devices are presented in Sections VI and VII, respectively. Section VII concludes this paper.

II. PRELIMINARY

A. Dynamic Synapse

In human brains, synapses represent electrical and/or chemical communication links between neurons. It has been widely believed that the behavior of a biological synapse is a spatio-temporal process: a synapse is activated by input spikes from preneuron and transforms these spikes into decayed traces to post-neuron [25]. For example, the synaptic current from preneuron \( i \) to post-neuron \( j \) can be formulated through a popular \( \alpha \)-function [26], such as

\[
I_{ij}(t) = w_{ij} \cdot \int_{0}^{\infty} \alpha(s) S_i(t - s) ds
\]  

where \( w_{ij} \) is the static synaptic weight describing the strength of the connection from preneuron \( i \) to post-neuron \( j \). \( S_i(t) \) is the input spike-timing train from preneuron \( i \) which can be represented as

\[
S_i(t) = \begin{cases} 
1, & \text{if } t = t_{ij} \\
0, & \text{otherwise} 
\end{cases}
\]

where \( t_{ij} \) is the set of spiking times from preneuron \( i \). The \( \alpha \)-function can be defined as

\[
\alpha(t) = A e^{-t/\tau_s}
\]

where \( A \) is the maximum magnitude of the decayed trace. And parameter \( \tau_s \) is the synaptic time constant, which defines the duration of the decayed trace.

As can be seen, a dynamic synapse model contains two major factors: 1) the (static) weight representing the synaptic strength and 2) the dynamic function describing how a synapse is activated/deactivated by input spikes.

So far, the study of synaptic strength tuning mainly focuses on static weight \( w \). The tuning of synaptic strength has two important attributes: 1) LTP that represents a slow time constant strength potentiation after a synapse has received strong and positive stimulus from active connections and 2) LTD...
as an opposite process. The influence of LTP and LTD are strongly related to the spiking time, initial synaptic strength, and type of post-synaptic cells [27]. Another important property of biological synapses is their self-learning abilities, e.g., STDP [27]. Experiment on cultured hippocampal neurons showed that within a critical correlation time window, the post-synaptic spiking that peaked after synaptic activation caused LTP, whereas the post-synaptic spiking before synaptic activation, can result in LTD [27].

The synaptic weight modification is an important component in the learning process. The Hebbian rule and the delta rule are two popular learning algorithms in artificial neural network family. In the Hebbian rule, the synaptic weight between two neurons increase (decreases) when they activate simultaneously (separately). The delta rule, also called as least mean square method or Widrow–Hoff rule [28], further improves the training performance by utilizing the output signal of post-neuron as a feedback to minimize the error between the target and output signals. As the synaptic weight modifications are determined solely by current spike combinations, the Hebbian and the delta rules are considered as static learning algorithms.

In SNNs, supervised STDP rule can be regarded as an improved version of the Hebbian rule in temporal space as it considers the time correlation between the input and target spikes in modifying the synaptic weight. ReSuMe algorithm improves supervised STDP rule’s performance which can further minimize the temporal difference between the target and output spikes. Both STDP and ReSuMe are temporal learning algorithms and more details of its use in our case study shall be described in Section II-C.

B. Synapse Design in Neuromorphic Circuits

To develop brain-like computing system, people need to build synapse hardware instead of simulating them. Neuromorphic circuits tend to mimic biological models and employ the same operation flows in weighting, tuning, and learning processes [29]. Previously, SRAM, floating gates, capacitors have been used in developing synapses [30]. These designs are severely constrained by the parallelism scale and the implementation size [3], [4]. Another prominent trend is designing synapses and neurons in analog or mixed-signal format [31]. The process variations and signal fluctuation potentially have great impacts on the system performance, which, however, can be partially amortized by synapse’s learning ability [32].

The recently rediscovered memristor devices at nanometer scale [7] demonstrate synapse-like behaviors, offering a more efficient way to implement synapses. For instance, Snider [6] successfully realized LTP, LTD, and STDP in a TiO2 device controlled by pulse width modulators (PWMs). The similar function was obtained in Ag/Si memristor synapse too through time division multiplexing (TDM) [8]. Another example is 1T1R-based HfO2 synapse with pulse shape filters in pre- and post-neurons [9]. However, these synapse designs only contain the static weighting function. The temporal transformation has to be integrated into post-neuron. In a large network where a signal is directed to multiple synapses, however, it is difficult to well preserve shaped pulses through synapses, as shown in Fig. 1. So all these demonstrations require complicated neuron circuits and are at small scale. A compact dynamic synapse design that can be integrated into cross-point array is essential for large-scale SNNs.

C. Spiking Neural Network With Temporal Codes

In the brain, external events are represented as spatio-temporal patterns of neural activity [33]. How information is encoded, however, is still not very clear. Usually rate coding and temporal coding are adopted in system development. The rate coding paradigm assumes that information is represented by the frequency of spikes while the encoding scheme of temporal coding uses the exact timing of individual spikes [34]. Substantial empirical evidence in neurology supports the existence of temporal coding [35]–[38]. While there is evidence for both rate coding and spike-timing based coding in the biological nervous system, some experiments suggest that in the human retina, visual signals from 106 photoreceptor cells are projected to 106 retinal ganglion cells in a form of spike trains (temporal codes) through temporal encoding [39]. Then these spikes can be processed and learned through spike-timing-based recall and spike-timing-based learning processes [40]. In this paper, we take a temporal pattern learning task as a case study to examine the performance of MD synapse design. The following two main functions are required in the application.

1) Spike-Timing-Based Recall: In spike-timing-based recall, the synapse model changes the temporal weight of a synapse (e.g., activated or deactivated) through temporal transformation function, and enables the neural network to produce the desired temporal patterns. The static weights of synapses remain unchanged during the entire recall process.

In hardware implementation, two approaches usually are adopted to realize the spike-timing function. One attempt is to integrate the temporal transformation function into neuron so synapse only has a constant static weight. Complex neuron circuitry, such as PWM and TDM components, are required to provide precise timing controls of temporal transformation function and ensure the quality of signal even it is connected to multiple synapses [6], [8]. The other approach of realizing both transformation function and static weighting in synapse can greatly simplify the neuron scheme and alleviate the signal propagation issue. The unclear static weight and complex synapse design are main concerns of the approach.

2) Spike-Timing-Based Learning: In this paper, we used two spike-timing-based learning algorithms—supervised STDP1 and ReSuMe. In both algorithms, weight updating of a synapse is determined solely by its own weight and excitation signals at the current time step. Such a local spatio-temporal learning scheme can be easily added to hardware synapse network. Here, a simple structure of one synapse connecting two neurons is used as example.

In STDP learning process, the post-neuron is forced to fire the target spike train $S_i(t)$. If an input spike $S_i(t)$ from the

1In the rest of this paper, we refer STDP to supervised STDP learning rule for simplicity.
signal window the synaptic weight increases. In contrast, a connection of two window titions. (a) STDP learning rule. (b) ReSuMe learning rule.

preneuron occurs within a predefined positive correlation time window ($T_{\text{Pcorr}}$) before $S_i(t)$, such as $0 \leq \Delta t = S_i(t) - S_o(t) < T_{\text{Pcorr}}$, implying the two neurons have a positive correlation, the synaptic weight increases. In contrast, a connection of two negative correlated neurons within a negative correlation time window ($T_{\text{Ncorr}}$) shall be weakened. Among a variety of STDP curves [41], Fig. 2(a) is a typical dependence of the synaptic weight change rate on $\Delta t$. The learning efficacy of STDP greatly relies on the correlation of the input and target spikes. When a target spike is uncorrelated to any of the input spikes, the STDP learning process fails. Thus, many input neurons firing at various patterns help increase the learning capacity of neural networks.

Unlike STDP, the ReSuMe learning rule requires output spikes to participate in the learning process and introduces a cost function to minimize the error between the target and output spikes. As illustrated in Fig. 2(b), input spikes are first converted to decayed traces through transformation function and then combined with the target spikes. The output spikes from post-synaptic neuron will be backpropagated to assist the weight updating. As such, the change of synaptic weight $w$ from preneuron $N_i$ to post-neuron $N_o$ can be described as follows:

$$\frac{d}{dt} w(t) = [S_i(t) - S_o(t)] \left[ a_i + \int_0^{\infty} \alpha(s) S_i(t - s) ds \right]$$

where $a_i$ is a constant that helps speed up the learning process, and $\alpha(t)$ is the prementioned $\alpha$-function that converts spike signal $S_i(t)$ to decayed traces. Equation (4) implies that the synaptic weight $w$ is updated when $S_i(t) \neq S_o(t)$. The direction and magnitude of the weight tuning are determined by the sign of $S_i(t) - S_o(t)$ and the convolution term $\alpha(t) * S_i(t)$, respectively.

III. MEMRISTOR-BASED SPATIO-TEMPORAL SYNAPSE

In this paper, we propose a dynamic synapse design by leveraging memristor technology. It supports both static weighting and dynamic temporal transformation function. So we name it as MD synapse. Note that the discussion in the work is limited to positive weights because a memristor, as a physical device, can represent only a positive value. Our previous work proved that a negative value can be obtained by combining two or more memristor devices [32].

A. Design Concept

The objective of this paper is to realize the following two types functions in synapse design.

1) Spatial weighting that modulates a spike through synapse. The static weight is tunable and adjustable in learning process whereas remains unchanged in recalls. In our design, one memristor is used to store the weight.

2) Temporal transformation function if a synapse is activated (ON) or deactivated (OFF), which is determined by the spiking times of pre- and post-neurons in learning/recall process. This is realized by a second memristor in MD synapse, which turns on only when the pre- and post-synaptic spikes arriving at proper timings. If the timing is incorrect, it remains turned off, preventing transmission of signals to the post-neuron.

Fig. 3(a) depicts an MD synapse design which is composed of two memristors ($M_1$ and $M_2$) and one resistor ($R$). $M_1$ realizes the temporal transformation and the conductance of $M_2$ ($G_2$) represents the static weight. For ease of explanation, we assume $M_1$ and $M_2$ have an identical device structure. Therefore, they have the same ON and OFF resistance states ($R_{\text{ON}}$ and $R_{\text{OFF}}$) and the identical switching dynamics. Note that the proposed MD synapse design can be generalized by applying different memristors with different characteristics to $M_1$ and $M_2$, as we shall discuss in Section VII-A.

To protect the static weight $G_2$ in recall, we connect $M_2$ with resistor $R$ in parallel so that the majority of the voltage across the synapse applies to $M_1$. Accordingly, the following inequality corresponding to the worst-case situation when $M_1$ and $M_2$ are, respectively, at ON and OFF states shall be satisfied:

$$R_{\text{ON}} > R_{\text{OFF}} \cdot R/(R_{\text{OFF}} + R).$$

(5)

Assume $R_{\text{OFF}} = k \cdot R_{\text{ON}}$ and $R = x \cdot R_{\text{ON}}$, (5) turns to $k + x > kx$, which indicates that $x \leq 1$ shall be satisfied because $k > 1$. Here, we set $x = 1$ and make $R = R_{\text{ON}}$. By adjusting the voltage across the synapse, $M_1$ can be switched alone without impacting $M_2$. The state change of $M_2$, however, is always associated with $M_1$’s switching.

Fig. 3(a) also illustrates the cross-sectional view of an MD synapse structure: $M_2$ and $R$ are isolated by a thin insulator and stacked above $M_1$. The structure is very similar to a double layer resistive random access memory device. The layout in Fig. 3(b) shows that MD synapse has an area of $8F^2$, where $F$ represents the technology feature size. Very importantly, the two-terminal structure can be easily integrated into cross-point arrays that have been widely investigated and explored for high-density synapse networks.

B. Characterization of MD Synapse

The proposed MD synapse generally is suitable for many types of memristor technologies. In the work, we adopted an experimentally calibrated model based on TaO$_x$ devices [24].
TaO$_x$ has been identified by HP Labs as one of the most promising memristor material for high density, low power, high endurance, and fast sub-ns programming [7], [42], [43]. Though TaO$_x$ devices in nanometer dimension have been demonstrated [44], [45], we use the micrometer device model [24] in the following simulations for it is more mature and accurate at the current stage. The design concept of our synapse, however, can be extended to nano-devices.

Fig. 4 shows the I-V characteristic of the TaO$_x$ device model. A sufficient positive SET pulse (negative RESET pulse) makes the TaO$_x$ device switch toward ON (OFF) state. The SET/RESET switching threshold changes with the sweeping time, which has been considered in our simulations.

1) DC Response: We analyze the I-V characteristic of MD synapse and show the simulation results in Fig. 3(c). The corresponding I-V curves of $M_1$ and $M_2$ during the operation are also included for reference. Obviously, when the voltage across the synapse is too small to meet TaO$_x$ device’s SET/RESET threshold under a given sweep time, neither $M_1$ nor $M_2$ can change. As the synapse voltage increases gradually, $M_1$ will first reach its switching condition. The top three I-V curves in Fig. 3(c) demonstrate that the dynamic component $M_1$ can be freely switched ON/OFF while the static component $M_2$ remains unchanged. The bottom three I-V curves in Fig. 3(c) implies that an even larger voltage amplitude is required to trigger the two-stage switching behavior including both $M_1$ switching and $M_2$ weight tuning.

In brief, a positive excitation that only set $M_1$ will enable the synaptic weighing function, while a negative excitation that only reset $M_1$ will disable the weighting function by putting the synapse back to high resistance state. To tune the weight of an MD synapse, the amplitude of the applied voltage shall be sufficiently large to switch $M_1$ and tune $M_2$.

2) Response to Spiking Excitation: For its high scalability and energy efficiency, SNN is good for large-scale neuromorphic implementation [4]. Instead of the complex synaptic signals in modulated format illustrated in Fig. 2, simple square pulses can be used for MD synapses as the input spikes at pre-neuron and the output spikes at post-neuron. To be consistent with TaO$_x$ operation, we use SET/RESET pulses to represent the positive/negative voltage across an MD synapse.

Fig. 5 summarizes the state transition diagram of MD synapse by varying SET/RESET pulses at different voltage amplitudes.

The pulse duration is fixed at 500 ps. For example, when $M_1$ is ON, a RESET pulse with an amplitude between 1.1 and 1.6 V can reset $M_1$ to OFF without changing $M_2$’s state; if the RESET pulse is larger than 1.6 V, not only $M_1$ will be reset to OFF, but also $M_2$ can be tuned toward OFF.

Considering that the dynamic component $M_1$ is either ON or OFF$^2$ while the static component $M_2$ could be unchanged (NC), tuning to ON, or tuning to OFF, a synapse has six possible transition states. Based on the analysis in Fig. 3(c), the situations of “$M_1$ ON and $M_2$ is tuning to OFF” and “$M_1$ OFF and $M_2$ is tuning to ON” can never occur and hence are excluded. Notably, $M_2$’s tuning rate is not a constant.

$^2$For simplicity, we refer $M_1$’s ON/OFF state as the MD synapse state in the rest of this paper.
value but determined by the present dynamic state and static weight of synapse as well as the applied voltage.

IV. SYNAPTIC FUNCTIONS OF MD SYNAPSE

In this section, the synaptic properties of MD synapse including the spike-timing-based recall and synaptic weight tunability will be examined and verified. Furthermore, STDP as the fundamental spike-timing-based learning rule will be applied to study MD synapse’s learning characteristics. MD synapse could operate with pulses of milliseconds width to mimic the biological synapse behavior; however, to pursue the performance potential, we use subnanoseconds pulses to demonstrate its functionalities. By integrating both transformation function and static weighting into synapses, neuron’s interface can be simplified as spikes rather than precisely shaped pulses, as shown in Fig. 1. This also reduce the circuit design complexity of the neurons. Moreover, spikes signals are easier to propagate among a large scale of neural networks comparing to shaped pulses, thus MD synapse can also alleviate the signal propagation issue.

A. Spike-Timing-Based Recall

In a spike-timing-based recall, $M_1$ switches ON or OFF based upon the timing of pre- and post-spikes, performing a simple dynamic temporal transformation function. Accordingly, the synapse is activated or deactivated. Pulse shape modulator is not required because the pulse shaping effect is achieved through SETting/RESETing $M_1$. For instance, Fig. 6(a) shows that a prespike from the preneuron initializes a positive SET pulse through the synapse, making it activated. A post-spike from the post-neuron results in a negative RESET pulse, which eventually deactivates the synapse. The static component $M_2$ remains at its initial value during the entire procedure.

A low dc signal of 0.2 V is as the background signal in recall to support the transformation function. And the static weighting is reflected by the overall volume of charge through the synapse. Once a prespike arrives and enables $M_1$, we start to track the accumulated charge. The assessment continues until a post-spike disables $M_1$.

There are three types of typical timing situations in spike-timing-based recall. We examined and studied the MD synapse behavior for each case separately.

Case 1: The preneuron fires much faster than the post-neuron, forming a multispike train with many SET pulses followed by a few RESET spikes. The MD synapse behavior under such a condition is shown in Fig. 6. $M_1$ turns ON at the first SET pulse and remains ON until a RESET pulse comes. Because of the over-tune induced memristance shift [46], the conductance of $M_1$ could increase further if two SET pulses fire in consequence. Even though, $M_1$ can still be switched OFF by extending the duration or number of RESET pulses. Notably, during the entire recall process, the resistance of $M_2$ remains constant and determines the total charge through the synapse. More specific, the charge accumulation is faster when $M_2$ is $R_{ON}$ but much slower if $M_2$ is $R_{OFF}$.

Case 2: When the pre- and post-neurons are strongly correlated, their firing events occur alternatively and appear as a sequence of SET/RESET pulses through the synapse. Under the circumstance, $M_1$ (and the synapse) switches between ON and OFF states but $M_2$ is not affected, as shown in Fig. 7. The charge accumulation through the synapse is at a low rate...
when the synapse is OFF but increases significantly once the synapse turns on. This process is robust and repeatable.

Case 3: A backward multispike train is generated when the burst of the post-neuron is much faster and more frequent than that of the preneuron. As the opposite situation of case 1, the spike-train through the synapse is in a form of many RESET pulses followed by several SET pulses. During the sequence of RESET pulses, the synapse is OFF and thus not much charge can pass through it. Certainly, $M_1$ can be reactivated by any SET pulse and $M_2$ remains intact.

B. Weight Tunability

As the basis of learning process, the weight tunability of MD synapse including LTP and LTD was examined. Note that the tuning targets at only the static weight of $M_2$, not for $M_1$ that represent the activation status of the synapse. As shown in Fig. 5, spikes with large amplitude at the pre-/post-neurons (or strong SET/RESET pulses) enable the tuning process.

For ease of explanation, we give an example shown in Fig. 9. Assume a strong correlation exists between pre- and post-neurons. They fire alternatively, appearing as a sequence of SET/RESET pulses through the synapse. In the first ten cycles, the spikes generated at preneuron is stronger. As a result, $M_2$ gradually shifts toward ON state with better conductivity, successfully demonstrating the LTP feature. The scenario in the following ten cycles is opposite: the stronger spikes at the post-neuron makes the RESET procedure more efficient. Thus, the effective conductance of $M_2$ when the synapse turns ON gradually reduces, implying an LTD behavior. The change of MD synaptic strength (conductance) is reflected by the charge passed through the synapse, as shown in Fig. 9(c). In summary, the positive stimuli corresponding to stronger-SET/weaker-RESET combination enables LTP feature. And the LTD can be realized under the circumstance of weaker-SET/stronger-RESET pulses, implying negative stimuli. Note that $M_1$ takes majority of pulse voltages and hence always reach ON or OFF state. In contrast, $M_2$’s conductance slowly changes because only a small amount of voltage applies on it.

As seen in Fig. 9(b), the conductance of the synapse increases in “steps” and decreases in “hops.” This is because a constant SET voltage $V_{\text{SET}} = 1.7$ V is applied in all the cycles. The conductance of synapse is always increases by a SET pulse and then decreased more by a RESET pulse. We particularly selected and presented this fast timing setting to investigate the performance limitation of TaO$_x$ devices. Moreover, an asymmetric tuning curve of $M_2$ can be observed. It takes ten pulses to sweep $M_2$ from OFF to ON, while the switching in the opposite direction is much slower due to intrinsic switching asymmetricity in TaO$_x$ devices [24].

C. STDP Learning

As an improved version of the Hebbian learning rule at temporal space, STDP learning rule can be taken as a causality detector. Correlation time window of a spike is used to evaluate its causality with other spikes: if a prespike fires before (after) a post-spike within the correlation time window, the synaptic strength of the synapse in between shall be potentiated (depressed), corresponding to an LTP (LTD) behavior. Here STDP learning rule is supervised so the post-spike is forced to fire at the target spike pattern.

Fig. 10 shows the realization of STDP learning by employing MD synapse under these two conditions. Here, a prespike is followed by a small dc signal of 0.4 V lasting for $T_{\text{corr}}$, representing the positive correlation time window of the spike. The negative correlation time window $T_{\text{Ncorr}}$ can be formed by setting a normal RESET pulse $T_{\text{Pre}} - T_{\text{Ncorr}}$ ahead of the post-spike. In this way, synapses for uncorrelated input spikes are predeactivated and will not be affected. Since a natural $T_{\text{Ncorr}}$ has been naturally defined by the time between previous post-spike and the current prespike in the design, a separate setting of $T_{\text{Ncorr}}$ can be saved.

Fig. 10(a) illustrates the scenario when the prespike injects first and the corresponding post-spike falls within $T_{\text{Pre}}$. Fig. 10(b) illustrates the scenario when the post-spike injects first and the corresponding prespike falls within $T_{\text{Pre}}$.
the prespikes. Though the strong SET pulse(prespike) remain unchanged, the small dc signal associated with the prespike degrades the strong RESET pulse(post-spike) to a normal RESET. Such a condition makes the $M_2$ conductance increase, resulting in an LTP process. The simulation results match well with our previous analysis in Section III-B. The realization of LTD process is shown in Fig. 10(b), where the RESET pulse (post-spike) remain strong and has larger impact.

Causality decision is not the only important criteria of a synapse’s STDP learning ability, which is also determined by the amplitude, time and shape of spikes as well as the initial synaptic weight. We characterize the learning efficiency of an MD synapse. The characterization is conducted by applying two recall cycles, respectively before and after an STDP learning cycle (either LTP or LTD) at different pre-/post-spike configurations [27]. The learning efficiency is measured by the change of effective synapse conductance (activated) in the two recalls.

The results in Fig. 11 show that for LTD, the change rate of synapse conductance increases as the initial state of synapse is more conductive. This reflects the $M_2$’s switching feature from ON to OFF, as shown in Fig. 9(b). The LTP, however, demonstrates an interesting convex curve. It implies that during $M_2$’s switching process from OFF to ON, its conductance changes faster at the beginning and then slows down as the device finally turns saturated at a full ON state. The difference in LTD and LTP characterization is resulted by the asymmetric switching of TaO$_x$ memristor.

D. ReSuMe Learning

ReSuMe learning rule is the temporal version of delta learning rule. It has better learning quality than STDP since it uses the free post-spikes as feedback to minimize the error between target spikes and post-spikes.

We use the example in Fig. 12 to illustrate the ReSuMe learning ability of MD synapse. Similar as STDP learning, a small dc signal with a period of $T_{corr}$ following a prespike is used to represent its correlation time window. However, based on the requirement of ReSuMe, the dc signal shall terminate right away when post-spike is generated. Thus, the convolution term $a_d(t) * S_i(t)$ of the original ReSuMe algorithm in Fig. 2 can be represented by the synaptic current excited by the prespikes and the following dc signals. The given example presents four typical situations.

1) There is no prespike. Since target spike is lower than SET threshold, MD synapse remains at OFF state. Neither the target spike nor the post-spike can change the synaptic conductance.

2) The target spike happens before the post-spike, and both of them fall into the correlation window of the prepulse. As such, the post-spike performs as a normal RESET and causes an LTP process.

3) Similar to scenario 2), however, the post-spike happens before the target spike. The post-spike tunes $M_2$ toward OFF state, implying an LTD process. Under this situation, the target spike does not contribute to the learning process because it cannot SET the device alone while the dc signal has already been terminated by post-spike.

4) The target spike and post-spike are approximately synchronized. There is no update on $M_2$, the synapse keeps at ON and the dc signal applies. Note that the design even do not require a perfect matching of the target spike and post-spike because memristor state change requires SET/RESET pulse last for sufficient time.

There are two situations missing in Fig. 12. When the target spike is uncorrelated to the prespike, it will not affect the synaptic weight at all. Or, if the post-spike does not
to convert any static pattern into spatio-temporal patterns as the function of the LIF neuron can be simplified as follows. The temporal encoding method (Section II-C) was applied between the learning cycles. Particularly, we examined the synaptic conductance in ON state. With larger post-spike as RESET, the LTP and LTD curves shift down linearly. Therefore, ReSuMe exhibits the better learning characteristics than STDP—better linearity of peak current change rate and more flexible state modification.

Interestingly, both STDP’s and ReSuMe’s learning characteristics obtain the similar trend as the observation in biological synapses: LTP shows a linear decreasing trend with synaptic strength’s increment, while LTD is not strongly relevant with initial synaptic strength [27]. For TaOx-based MD synapse, ReSuMe’s LTP behavior has a better linearity than STDP’s, while the characterization of LTD demonstrates an opposite trend. This can be explained by the intrinsic asymmetric ON and OFF switchings of TaOx devices [24].

V. MD SYNAPSES IN SPIKE-TIMING NEURAL NETWORK

A. Application Setup

We demonstrate the use of MD synapses in SNN by adopting a case study from [20]. The selected neural network is trained on a random target firing pattern of 400 ns. As shown in Fig. 14, 400 synaptic inputs go through 400 MD synapses and then are collected by a leaky integrate-and-fire (LIF) neuron. The temporal encoding method (Section II-C) was applied to convert any static pattern into spatio-temporal patterns as the input spiking trains $S_{i1}$-400$(t)$ in the given study case. If MD synapses have been properly trained, the fire pattern of the output neuron $S_o(t)$ shall converge to the target firing pattern $S_t(t)$.

To accommodate the easy timing control of MD synapses, the function of the LIF neuron can be simplified as follows.

1) The charge at the LIF neuron is leaking at a constant speed of $Q_{\text{leak}}$.

2) The LIF neuron fires whenever its accumulated charge exceeds the firing threshold, i.e., $Q > Q_{\text{th}}$.

For ease of comparison, we adopt the same assumption in [20] that each synaptic input fires only once during the single presentation of the target signal. And the particular input pulses are distributed uniformly throughout the 400 ns time interval. The conductances of 400 MD synapses are initialized randomly by applying a Gaussian distribution to $M_2$ conductance. All the synaptic inputs are limited to excitatory because the MD synapses based on real physical devices does not provide negative weights. Table I summarize the signal setup in recall and learning processes.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>SIGNAL SETUP FOR SNN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{STDP}}$</td>
<td>$V_{\text{RESET}}$</td>
</tr>
<tr>
<td>Recall</td>
<td>1.1V</td>
</tr>
<tr>
<td>STDP</td>
<td>1.7V</td>
</tr>
<tr>
<td>ReSuMe</td>
<td>1.1V</td>
</tr>
</tbody>
</table>

B. Learning Temporal Patterns Using STDP

The STDP learning rule was applied to the given application. As illustrated in Fig. 14(a), during the learning process, the LIF neuron is forced to fire at the target pattern $S_t(t)$. Fig. 15(a) shows the progress of 60 learning cycles, each of which last 400 ns. Within each learning cycle, the target pattern $S_t(t)$ fires at the designed time illustrated by $\circ$ in the figure. After each learning cycle, we conduct a recall and record the output pattern $S_o(t)$ as $\times$. The simulation results show that overall $S_o(t)$ tends to approach $S_t(t)$ but it is not always successful. This is due to the intrinsic drawback of STDP learning rule: the output of neuron does not participate in the learning process. So sometimes the difference between $S_t(t)$ and $S_o(t)$ cannot be minimized.

Fig. 15(b) compares the conductance of the 400 MD synapses at the initialization (blue curve) and after 60 cycles of learning (red bars). At the end of learning process, most synapse are saturated at conductance boundaries. This is mainly because STDP learning rule requires relatively large synaptic weight range [47]. The scenario also implies that the constrains of physical memristor devices could greatly affect the learning performance. After all, a large range of memristance could improve the STDP learning performance.
Error minimization between STDP and ReSuMe. Different from STDP, the ReSuMe learning rule includes both amplitude and period of the excitation, an error margin in learning process. Since the memristor state change relies on learning of the given design using ReSuMe learning rule.

C. Learning Temporal Patterns Using ReSuMe

Similarly, we examined the effectiveness of temporal learning of the given design using ReSuMe learning rule [20]. Different from STDP, the ReSuMe learning rule includes the error minimization between \( S_t \) and \( S_o \). As shown in Fig. 14(b), \( S_t \) is combined with every synaptic input signal \( S_t \) to generate \( S_o \) at the LIF neuron. The output pattern \( S_o \) is then fed back to every synapse to participate in the learning process. Since the memristor state change relies on both amplitude and period of the excitation, an error margin can be naturally formed between \( S_t \) and \( S_o \): whenever the target and the output pulses overlap, the rest of their pulse duration has little impact on the memristor state.

The learning progress of ReSuMe rule of the given example is shown in Fig. 16(a). In most test cases, the output pattern generated by the LIF neuron converges to the target pattern within 25 learning cycles, demonstrating a much successful learning ability. Moreover, the pattern learning tasks can be completed without observing synapse conductance saturation as shown in Fig. 16(b). It delivers an important information: even the MD synapse design based on TaO\(_x\) devices has limited synaptic conductance tuning range, it can still provide sufficient learning ability in neural network applications with assist of appropriate learning rules. Further increase of memristance range will alleviate the situation.

D. Energy Estimation

To evaluate the energy efficiency of MD synapses, we calculate the energy consumption per spike in recall and learning processes by the following:

\[
E_{\text{total}} = E_{\text{SET}} + E_{\text{ac}} + E_{\text{RESET}} \quad (6)
\]

where, \( E = V^2 T_s/R_\text{MD-synapse} \). \( T_s \) is the duration when the signal is applied. An additional energy consumption related to the target pulse \( E_{\text{TARGET}} \) shall be added into (6) in ReSuMe learning. Here, only the energy consumed on MD synapse is estimated. Based on the signal setup in Table I, the recall consumes only 14.6 pJ per spike and the energy consumption in learning process is 36.7 and 64.0 pJ per learning spike for STDP and ReSuMe, respectively. Note that the micro model of TaO\(_x\) devices used in this paper has a low resistance range of 70–670 \( \Omega \) [24]. Applying nano-scale devices can significantly increase the memristance value to 100 k\( \Omega \)–1 M\( \Omega \) [7] and further reduce energy consumption. For instance, the micro-scale TaO\(_x\) device needs >10 mA current to switch, but for the nano-scale device, the switching current will be at only \(~10\) uA level, which indicates a three orders of magnitude of energy reduction and the MD synapses could be operated at several fJs. Comparing to other analog synapse components, a nano-scale MD synapse can provide more complex weighting function with equal or less energy consumptions as well as simplify the neuron design [48].

VI. Nonideal Conditions in Implementation

Effectively connecting neurons is an essential requirement in neural network hardware implementation. For a fully-connected network with \( n \) neurons, the number of synapses is in an order of \( n^2 \). The memristor cross-point array illustrated in Fig. 3(b) is expected to provide the densest implementation and the best connectivity of synapse network. However, the nonideal conditions in circuit implementation, such as the device variations and signal degradation, may severely affect the system performance. The impacts on the MD synapse based cross-point arrays will be discussed in this section.

A. Impact of Device Variations

In the study, the variations of all the three devices within the MD synapse, including \( M_1 \), \( M_2 \), and \( R \), are considered in the experiment. We assume that the variation of each device follows a Gaussian noise distribution with \( \sigma \) up to 1%–10%. Fig. 17 presents the induced variations of \( V_{m1} \) and \( V_{m2} \) (the voltages across \( M_1 \) and \( M_2 \), respectively) under two worst-case scenarios.

1) In RESET process, \( M_1 \) is in ON state and \( M_2 \) is in O\( \text{F} \) state.

2) In SET process, both \( M_1 \) and \( M_2 \) are OFF.

As aforementioned, to ensure the proper function of MD synapse, \( M_1 \) shall always have a higher switching priority than \( M_2 \). Accordingly, the device variation \( \sigma \leq 6\% \) is tolerable in MD synapse design. As \( \sigma \) is greater than 6%, it is possible that \( V_{m1} \) is lower than \( V_{m2} \) in RESET process, violating the operation condition of MD synapse.

B. Impact of Signal Degradation

In a typical cross-point array structure, the signal degradation is mainly affected by two factors: the most conductive unselected devices which sink a large portion of current flow (so called as sneak current), and the resistance of metal wires used in cross-point array. More specific, the ratio of the ON state resistance of the cross-point devices over the wire segment resistance \( R_w \) limits the array scale [49].

Fig. 18 shows the effective voltage of cross-point device normalized to the input pulse voltage under the worst-case operating condition defined in [49]. For a conventional cross-point array with a TaO\(_x\) memristor as the cross-point device,
$R_{ON}/R_w \approx 100$. To ensure that the furthest corner device can reach at least 60% of the input voltage signal, the array size cannot exceed $8 \times 8$. When developing the cross-point array with the MD synapse design, the lowest resistance bond of unselected (deactivated) MD synapses is

$$\min R_{\text{cross-point}} = R_{M1,\text{OFF}} + \frac{R \cdot R_{M2,\text{ON}}}{R + R_{M2,\text{ON}}}$$  \hspace{1cm} (7)$$

where $R_{M1,\text{OFF}}$ is the resistance of $M_1$ in OFF state, and the second term on the right side represents the parallel resistance of $R$ and $M_2$ in ON state. For a TaO$_x$-based MD synapse with the given device parameters, $\min R_{\text{cross-point}}/R_w \approx 1000$. As seen in Fig. 18, the array size can be extended to $32 \times 32$. Moreover, if different types of memristor technologies can be applied to $M_1$ and $M_2$ so as to increase $R_{M1,\text{OFF}}$, $\min R_{\text{cross-point}}$ can further increase. The scale and performance of MD synapse can dramatically improve.

VII. MEMRISTOR DEVICES IN MD DESIGN

A. MD Synapse With Two Different Memristors

In original MD synapse design, two identical memristors are employed so a resistor $R$ is needed to protect $M_2$ in recall process. Utilizing two different types of memristor devices for $M_1$ and $M_2$ and eliminating the parallel resistor can result in a more efficient design from two aspects.

1) The MD synapse structure is simplified to two memristors connected in series. The unit area of a synapse decreases to $4F^2$ so the fabrication cost reduces.

2) When $M_2$ is not forming free, the difficulty in $M_2$’s forming process lowers.

If both memristors are voltage controlled, their device parameters, including the low resistance states ($R_{ON}$), high resistance states ($R_{OFF}$), SET voltage amplitudes ($V_S$), and RESET voltage amplitudes ($V_R$) shall satisfy the following constrains:

$$V_{M1,S} \leq \frac{R_{M1,ON}}{R_{M1,ON} + R_{M2,OFF}} V_{\text{recall}} \quad \text{when SET } M_1$$

$$V_{M2,S} > \frac{R_{M2,OFF}}{R_{M1,ON} + R_{M2,OFF}} V_{\text{recall}} \quad \text{when SET } M_1$$

$$V_{M1,R} < \frac{R_{M1,ON}}{R_{M1,ON} + R_{M2,OFF}} V_{\text{recall}} \quad \text{when RESET } M_1$$

$$V_{M2,R} \geq \frac{R_{M2,ON}}{R_{M1,ON} + R_{M2,OFF}} V_{\text{recall}} \quad \text{when RESET } M_1.$$  \hspace{1cm} (8)

Here, $V_{\text{recall}}$ is the pulse amplitude used in recall process. The first two constrains correspond to the worst-case condition when setting $M_1$. And the last two constrains describe the worst-case condition in resetting $M_1$. In a recall process, $M_2$ shall always keep intact. Fig. 19 shows these constrains in a graphic view. The gray area represents the working region that satisfies (8). $X$ and $Y$ specify the boundary conditions.

$$X = \frac{R_{M2,ON}}{R_{M1,ON}} \quad \text{and}$$

$$Y = \frac{R_{M2,OFF}}{R_{M1,OFF}} \frac{V_{M2,R}}{V_{M2,S}}.$$  \hspace{1cm} (9)

and the optimal configuration of $M_1$ and $M_2$ shall obey the following relations to maximize the resistance ratio between $M_2$ and $M_1$:

$$\frac{R_{M2,ON}}{R_{M1,ON}} \leq \frac{V_{M2,R}}{V_{M1,R} + V_{M2,S} - V_{M2,R}}, \quad \text{and}$$  \hspace{1cm} (10a)

$$\frac{R_{M2,OFF}}{R_{M1,OFF}} \leq \frac{V_{M2,S} - V_{M1,R}}{V_{M1,R}}.$$  \hspace{1cm} (10b)

The two independent inequalities of (10) define the relation of $M_2$’s four parameters. For instance, with the assumption of $V_{M1,R} > V_{M1,S}$, the SET process of $M_1$ does not appear as the worst case to constrain the design, implying $V_{M1,S}$ does not have a strict requirement. In general, relatively low switching voltage and high resistance range are preferable for $M_1$. The high SET voltage and low RESET voltage are more important for $M_2$ to improve the effective OFF/ON ratio and therefore get better synapse performance. Here, the effective OFF/ON ratio corresponds to the range of memristor resistance states to promise proper functionality of MD synapses.
In the case of current-controlled memristor devices, we can remove the resistor to let the same amount of current passes through $M_1$ and $M_2$. In order to remain the state of $M_2$ intact when switching $M_1$ ON/OFF, $M_2$ shall be able to tolerate a larger switching current than that of $M_1$.

### B. Use of Memristors With Volatile Switching

Memristor is usually regarded as a nonvolatile device. However, the retention loss has also been observed in WO$_x$ and Ag$_2$ memristors under low and short pulse excitations [10], [11]. This indeed can be taken as a form of volatile switching, meaning, after a memristor switches its state, the conductance drifts back to the original state (or certain states) within a time scale from nanoseconds to minutes. In single-memristor based synapse designs, the volatile switching behavior has been linked to the STP [22], [23]. Opposite to LTP, STP describes the phenomenon in nervous system that under small excitations, synapse strength rises and then decays to the original value after the excitation is removed.

The proposed MD synapse contains two memristors. The volatile switching behavior of $M_2$, if any, can also be related to STP as $M_2$ represents the spatial weight of synapse. If $M_1$ demonstrates the volatile switching behavior, the temporal transformation function of the synapse will be affected. As a simple illustration, let us assume $M_1$’s conductance exponentially decays over time after a volatile setting. It has two important design implications. First, solely utilizing the dc signal on synapses after SET pulse may be able to form a more complex and accurate transformation function, e.g., $\alpha$-function in (3). Second, as $M_1$ can turn itself off, the RESET pulse from post-neuron will be no longer needed. The neuron design complexity can be further reduced.

### VIII. Conclusion

In this paper, we present an MD synapse design. By adopting the latest experimentally grounded TaO$_x$ model, we characterize its electrical properties and synaptic features. The simulation results show that the design can enriches the synaptic functionalities in temporal recall and learning abilities. Meanwhile, the design complexity of neurons can be significantly reduced. Furthermore, we perform a temporal pattern learning task by utilizing STDP and ReSuMe learning rules, to demonstrate the usage of MD synapse in SNNs. Our result shows recall and learning ability in nano-second scale. The average recall energy is merely 14.6 $pJ$ per recall spike. And the learning energies when utilizing STDP and ReSuMe are 36.7 and 64.0 $pJ$ per learning spike, respectively. Comparably, the ReSuMe learning rule achieves better accuracy and faster learning speed than the STDP learning rule. The dependency on the constraints of memristor device physical parameters is also more relaxed when utilizing the ReSuMe learning rule. In addition, the simple structure of MD synapse naturally supports the integration of cross-point arrays and alleviates the complexity of the associated neuron design. These promising features make the hardware implementation of massive SNNs closer to reality.

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