HS3-DPG: Hierarchical Simulation for 3-D P/G Network

Yu Wang, Song Yao, Shuai Tao, Xiaoming Chen,
Yuchun Ma, Yiyu Shi, and Huazhong Yang

***Abstract*— As different tiers are stacked together in 3-D integrated circuits, the power/ground (P/G) network simulation becomes more challenging than that of 2-D cases. In this brief, we propose a hierarchical simulation method suitable for 3-D P/G network (HS3-DPG), which takes advantage of the inherent hierarchical structure of 3-D P/G network. The port equivalent model (PEM) is introduced to mask the details of P/G grid in each tier. Besides, we introduce the locality property to further simplify the simulation. Some 3-D P/G network benchmarks extracted from industrial designs are used to verify the correctness of our method. Experimental results show that, HS3-DPG can achieve considerable speedup, while maintaining high accuracy. Simplified PEMs considering the locality property can save nearly 80% memory allocation compared with the full PEMs when the number of through-silicon-vias between the adjacent tiers becomes quite large.**

***Index Terms*— 3-D power/ground (P/G) network, hierarchical simulation, locality property, port equivalent model (PEM).**

I. Introduction

With the feature size shrinking, traditional electronic design methodologies face some bottlenecks, such as per wafer cost, large interconnect delay, and high leakage power. The 3-D integration has been regarded as a promising solution to mitigate these problems. The 3-D integrated circuits (ICs) stack separate tiers in the vertical direction and connect them using vertical connections such as through-silicon-vias (TSVs). Compared with traditional 2-D integration, the 3-D technology can provide many benefits, such as reduction in the interconnect wire length and improvement of memory bandwidth [1].

The power delivery network (PDN) design is considered as one of the most critical challenges in IC design as power supply levels have significant effects on circuit performance. Reduced supply voltage levels in the grid can increase the gate delay and harm the functionality of circuits, leading to timing violations, incomplete functionality, and even silicon failures [2]. Consequently, a rational design of the power/ground (P/G) network is quite necessary to maintain the power integrity and guarantee the proper circuit operation. However, P/G network analysis is time and resource consuming since millions of nodes may exist in one P/G network.

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Y. Wang, S. Yao, S. Tao, X. Chen, and H. Yang are with the Tsinghua National Laboratory for Information Science and Technology, Department of Electronic Engineering, Tsinghua University, Beijing 100084, China (e-mail: yu-wang@tsinghua.edu.cn; yaos11@mails.tsinghua.edu.cn; taoshuai168@163.com; chenxm05@mails.tsinghua.edu.cn; yanghz@tsinghua.edu.cn).

Y. Ma is with the Tsinghua National Laboratory for Information Science and Technology, Department of Computer Science and Technology, Tsinghua University, Beijing 100084, China (e-mail: myc@tsinghua.edu.cn).

Y. Shi is with the Department of Electrical and Computer Engineering, Missouri University of Science and Technology, Rolla, MO 65409 USA (e-mail: yshi@mst.edu).

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Researchers have explored many techniques to accelerate P/G analysis for 2-D chips such as some multigrid-based approaches [3]–[5]. The multigrid method can accelerate the convergence of traditional iterative methods through interpolation between fine and coarse grids [6]. Yang *et al.* [7] extended a multigrid-based method called AMG-PCG to transient P/G network simulation. Besides, a memorized supernodal technique and some parallel forward and back substitution methods were also proposed in [8] and [9]. Furthermore, Zhao *et al.* [10] presented a hierarchical analysis approach for 2-D P/G networks using macromodels. The divide and conquer approach in P/G network analysis has a profound effect on researches of this area.

The P/G issues become much tougher in 3-D cases as power coupling between different tiers becomes tighter and the network scale may be several times larger than that of 2-D cases [11]. Recently, some techniques such as the extension of compact physical model [12] and the model-order-reduction methods [13] were proposed. However, the scalability cannot be ensured with those techniques. Hu *et al.* [14] suggested using standard reduced power models (SRPMs) to replace some tiers of 3-D P/G network that can also help to mitigate the conflict between data sharing and chip protection. Nevertheless, the key issue is how to build SRPM for each tier. A voltage propagation method for static 3-D P/G network analysis was proposed in [15]. However, the selection of the initial voltages has a large impact on the performance of their method.

In this brief, we propose a hierarchical simulation method, to accelerate 3-D P/G network (HS3-DPG) simulation in both static and transient cases without introducing much intrusiveness. The proposed method separates all tiers, extracts the port equivalent model (PEM) for each tier, reestablishes the global network with PEMs, and finally substitutes the global solution to compute voltages at inner nodes. To further simplify the PEM, we extend the locality effect in 2-D flip chips [16] to 3-D P/G networks.

The hierarchical simulation method is not a stand-alone approach. When the 3-D P/G network is separated into different tiers with additional dummy voltage sources, tiers are independent from each other, and thus existing techniques such as the AMG-PCG solver [7] and some parallelism simulators [8], [9] can be adopted to compute the PEM of each tier. Consequently, the proposed approach has a potential to explore a hybrid two-level parallelism in 3-D P/G network simulation. In this brief, we only evaluate the advantage introduced by the hierarchical method.

The main contributions of this brief are as follows.

1) We propose a HS3-DPG. The PEM is introduced to mask the details of the P/G grid in each tier and provide all information for interior communication. The PEM can also help to solve the intellectual property protection problem in 3-D IC design.
2) We explore different forms of PEM and evaluate their performance in static and transient simulation cases.
3) For the first time, we introduce the locality effect into the simulation of 3-D P/G network to further simplify the PEM.

The rest of this brief is organized as follows. Section II gives a brief overview of 3-D power delivery system model used in this brief. Section III illustrates our hierarchical simulation method. The locality property is introduced in Section IV and experimental results are presented in Section V. Finally, the conclusion is drawn in Section VI.

II. Modeling of 3-D Power Delivery System

A 2-tier example of the established circuit model of the 3-D power delivery system is shown in Fig. 1, which includes the

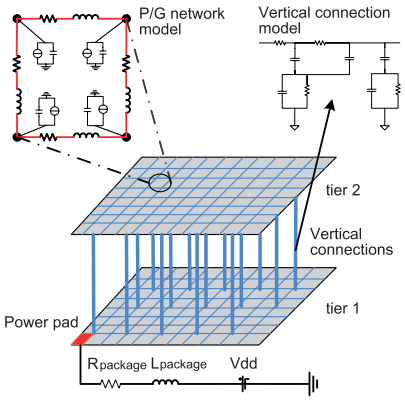

Fig. 1. Established circuit model of the 3-D PDN.

P/G network model, interconnect model, and simplified package model. The flip-chip package technology [16] is used in this brief. In 3-D power delivery systems, P/G TSVs connect the P/G networks in different tiers, and the bottommost tier (tier 1) is connected to the package through metal bumps and then routed to the voltage sources on the PCB board. Although all tiers are coupled together, the 3-D power delivery system still has an inherent hierarchical structure, which supports our hierarchical method in this brief.

The P/G network in each tier of 3-D power delivery systems in this brief is a mesh-based network. The circuit model of the P/G network on chip consists of current sources and the *RLC* model of P/G wires. The on-chip inductance effect is ignored when the frequency is <5 GHz [17]. In this brief, we determine on-chip parameters and wire segment dimensions through predictive technology model interconnect models under 45 nm technology [18].

The vertical bonding technology employed in this brief is face-to-back bonding, which means the vertical interconnect connects the back side of one tier and the face side of the other tier by tunneling through the substrate of one tier [1]. The circuit model of the vertical interconnect is adopted from [19].

In 3-D power delivery systems, clustered TSV topology and distributed TSV topology are commonly used [20]. In the clustered TSV topology, several TSVs are clustered together while aligned with C4 bumps in the bottommost tier. In the distributed TSV topology, TSVs are distributed individually. Compared with the distributed TSV topology, the clustered one can leave more continuous whitespace to logic circuits and ensure the manufacturability [21]. The clustered TSV topology is adopted in this brief.

As this brief focuses on the analysis of the on-chip part, the package model used in this brief is simplified as a lumped RL chain.

III. Hierarchical Simulation for 3-D P/G Network

In this section, we introduce the details of our hierarchical simulation method. First, the overall flow is presented. After that, the extraction method and properties of PEM are introduced. Furthermore, the detailed flow of the hierarchical transient simulation is illustrated.

A. Overall Flow of Hierarchical Simulation

The overall hierarchical simulation flow is shown in Fig. 2. With an entire 3-D P/G network, a preprocessor marks all the nodes connected to TSVs as ports and removes all the TSVs to separate the global network into tiers. With separated tiers, HS3-DPG first extracts the PEMs for every tier to replace the detailed grids. After that, TSVs are put back to connect all the PEMs and form a new global network. The

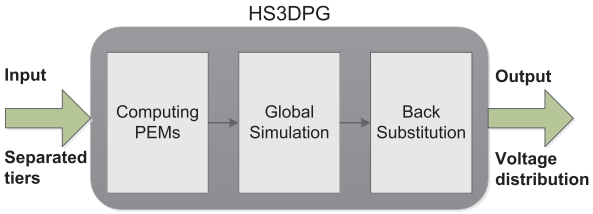

Fig. 2. Overall simulation flow of HS3-DPG.

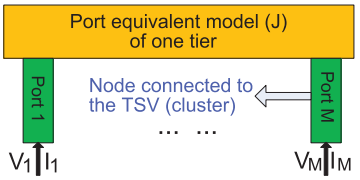

Fig. 3. PEM of one tier.

global network with PEMs has much fewer nodes than the original one, and thus becomes easy to simulate. Finally, HS3-DPG substitutes port voltages back into the P/G network in each tier and computes the inner node voltages.

A sparse Cholesky solver named CHOLMOD [22] is used in PEM extraction and back substitution phases of each tier. To solve an equation $Ax = b$, the CHOLMOD solver first decomposes the coefficient matrix A into LL^T and then executes back substitutions to obtain the solution. In the global network simulation, a recently released NICS-LU [24] simulator is adopted.

B. Port Equivalent Model

A simple denotation of one PEM is shown in Fig. 3. For one tier, the ports are defined as the nodes connected to TSVs (TSV clusters). As one TSV is connected to the metal layer through a μ-bump, which can be regarded as a super node, the port number of each tier is equal to the TSV (TSV cluster) number. The proposed PEM of one tier can be formulated as follows:

$$I = J * V + S = \begin{bmatrix} \frac{\partial I_1}{\partial V_1} & \cdots & \frac{\partial I_1}{\partial V_M} \\ \vdots & \ddots & \vdots \\ \frac{\partial I_M}{\partial V_1} & \cdots & \frac{\partial I_M}{\partial V_M} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_M \end{bmatrix} + \begin{bmatrix} S_1 \\ \vdots \\ S_M \end{bmatrix}$$

where M is the number of ports, $I \in R^{M\times 1}$ is the actual current vector flowing into this tier through these ports, $J \in R^{M\times M}$ is a Jacobi matrix reflecting port dependencies, $V \in R^{M\times 1}$ is the voltages at ports, and $S \in R^{M\times 1}$ is a current source vector attached to the ports in this tier. For circuit representation, each entry in the Jacobi matrix J is modeled as a voltage-controlled current source (VCCS). The PEM used here is similar to the multilevel Newton algorithm with macromodeling in nonlinear circuit analysis [25], while different from the macromodel used in [10]. The PEM for each tier and also each column of the Jacobi matrix J can be calculated all alone.

We illustrate how to use the PEM in our hierarchical method with an example shown in Fig. 4. The simple circuit in Fig. 4(a) with additional dummy voltage sources has only 4 nodes and connects with other tiers with 2 TSVs at nodes 1 and 2. Consequently, the corresponding PEM has 2 ports, which means 2 current sources and 2×2 VCCSs exist in the PEM circuit representation.

After separating all tiers, the PEM of one tier can be computed in six steps: 1) attaching dummy voltage sources (V_{dd1} and V_{dd2}) at

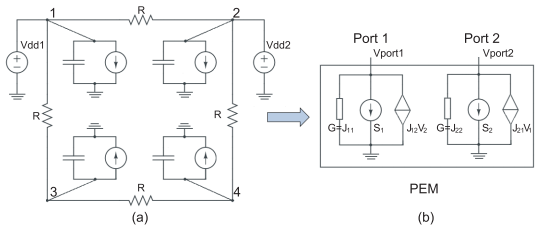

Fig. 4. PEM extraction when port number is 2. (a) Separated tier with two dummy voltage sources at ports. (b) Circuit representation of the corresponding PEM.

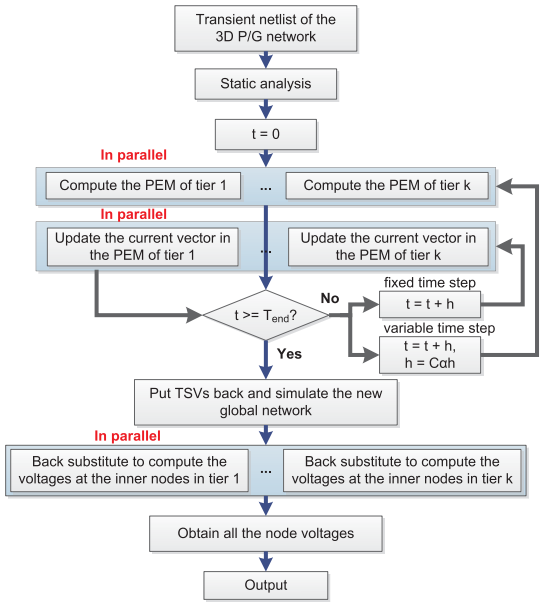

Fig. 5. Hierarchical transient simulation flow.

ports and forming an independent integral P/G network; 2) establishing the equation based on modified nodal analysis (MNA) method; 3) implementing the Cholesky decomposition operation; 4) attaching all ports to the ground ($V_{dd1} = V_{dd2} = 0$) and executing the Cholesky back substitution once to calculate the current source vector S; 5) assigning $V_{dd1} = 1$ V and $V_{dd2} = 0$, implementing the Cholesky back substitution, and then computing the current vector flowing into this tier through these two ports. This vector minus vector S is the first column of J, i.e., J_{11} and J_{21}; and 6) computing other entries of J and obtaining the full PEM. After the global simulation, the values of dummy voltage sources are assigned to exact voltages at ports ($V_{dd1} = V_{\text{port1}}$ and $V_{dd2} = V_{\text{port2}}$) and an additional Cholesky back substitution is executed to compute all voltages at inner nodes.

When the port number increases, the computing procedure is similar to the above. The only difference is that the number of ports to be scanned increases when obtaining the Jacobi matrix. As for the circuit representation, the number of VCCSs and current sources connected to each port increases accordingly.

C. Hierarchical Transient Simulation

The general flow of the hierarchical transient simulation is shown in Fig. 5. The proposed method first extracts the transient PEMs of all tiers for the entire time domain, then runs the global simulation with the transient PEMs, and finally back substitutes the global results into every tier. In the transient PEM, all entries of the current vector S are modeled as piecewise linear (PWL) sources. As the Jacobi matrix J in the transient PEM reflects port dependencies, which is unrelated to the dynamic current variation, it remains the same during the simulation when the time step is fixed. Otherwise, in the variable-time-step case, all entries of the matrix J in the transient PEM change all the time and are also PWL models.

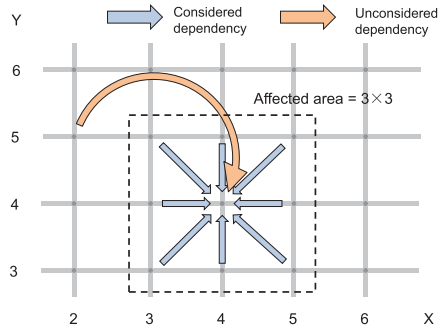

Fig. 6. In the simplified PEM which considers locality property, the dependencies out of the affected area of one port are not considered (each node in integer coordinates represents a TSV cluster).

When the time step is fixed, as matrix J in the transient PEM remains the same, only the current vector S needs to be computed every time step to update the PEM. According to the computing process of the PEM, the calculation of new current vector S at each step needs one Cholesky back substitution. Consequently, assuming there is n time steps, the overall time consumption of the hierarchical transient simulation consists of three parts: 1) the transient PEM extraction of each tier (one-time Cholesky decomposition at the first time step and n-time Cholesky back substitutions); 2) the global simulation; and 3) n-time final back substitutions. Meanwhile, the direct full simulation of the entire 3-D P/G network needs one-time Cholesky decomposition and n-time Cholesky back substitutions. Since the computation complexity of Cholesky decomposition is around $O(N^{1.5})$, postulating that there are k same tiers in the 3-D P/G network and considering the benefit from parallelism, the theoretical speedup of HS3-DPG in the fixed-time-step transient simulation is

$$\frac{T_{\text{Direct Solve}}}{T_{\text{HS3-DPG Trans}}} = \frac{Mk^{1.5} + nk}{M + 2n}$$

where $M = T_{\text{decomposition}}/T_{\text{back substitution}}$ is a large constant. According to the speedup formula, we can find that HS3-DPG is faster than the direct full network simulation as long as $k \geq 2$. Meanwhile, although the time consumption for one Cholesky back substitution is tiny compared with Cholesky decomposition, with the increase of n, the double n-time back substitutions of the hierarchical method still gradually decreases the speedup.

When the time step is variable, the time step should be updated following $h_{i+1} = C\alpha h_i$ at every step. The coefficient C ($0.8 \sim 0.9$) is a safety parameter and $\alpha = (e_{\max}/|E_{T,i}|)^{1/2}$, where $e_{\max}$ and $E_{T,i}$ are the max allowed error and the local truncation error in the last time step, respectively. As the time step h updates, the conductance matrix of the established MNA-based equation changes at every time step. Consequently, additional Cholesky decompositions are needed at every step.

IV. Simplified PEM

The number of VCCSs in the PEM increases with the square of the number of ports. Consequently, if there are a large number of ports, the PEM can be very complicated. To solve this problem, we introduce the locality property into the hierarchical simulation to simplify the PEM.

In the 2-D flip-chip packaging, frequently and uniformly distributed C4 bumps cause a locality effect, which means the current is

TABLE I
VERIFICATION OF THE HIERARCHICAL SIMULATION APPROACH IN STATIC ANALYSIS

Testbench			3D-μP (2 tiers)	3D-μPD (2 tiers)	3D-TxRx (3 tiers)
Direct full network simulation	Time (s)		0.72216	1.27565	0.24382
	Memory (MB)		72.46	89.12	20.22
HS3DPG	Time (s)	Compute PEMs	0.343403	0.635165	0.064954
		Compute the global network	0.004789	0.006003	0.012587
		Back substitution	0.009277	0.014926	0.005023
		Total Time	0.35742	0.65609	0.08256
	Memory (MB)	Compute PEMs	36.79	47.70	9.13
		Compute the global network	8.70	8.70	8.70
		Peak memory	45.49	56.40	17.83
	Speedup		2.021	1.944	2.953
	Maximum absolute error (V)		3.97e-12	4.26e-12	4.51e-12

TABLE II
RUNTIME COMPARISON OF THE FIXED-TIME-STEP TRANSIENT SIMULATION

Simulation time (ns)			1	10	20	50	100	500	1000	10000
Testbench	3-D-μP	Direct	1.617s	3.978s	6.061s	14.006s	25.239s	131.171s	245.136s	2215.605s
		HS3-DPG	0.841s	1.963s	4.644s	10.370s	21.553s	109.937s	216.354s	2057.201s
		Speedup	1.923	2.026	1.305	1.351	1.171	1.199	1.133	1.077
	3-D-TxRx	Direct	0.301s	0.732s	1.199s	3.120s	4.796s	22.547s	44.807s	453.641s
		HS3-DPG	0.173s	0.416s	0.701s	2.014s	3.111s	14.338s	28.430s	303.760s
		Speedup	1.739	1.760	1.710	1.549	1.542	1.572	1.576	1.493

generally drawn from the closest bumps for a particular area and the affected area of one power source in flip-chips is very limited. By implementing the locality effect, fast power grid analysis and design can be achieved [16].

In the 3-D P/G network, TSV clusters play the role of C4 bumps in the intermediate tiers. We can find that the influence of one TSV cluster on the others attenuates very quickly after passing through several clusters; the locality effect also exists in each tier of 3-D P/G network. Consequently, the port dependencies between TSV clusters that are far from each other can be ignored without introducing large error. Considering this, we can control the area that one TSV cluster can affect in the PEM; the dependencies between a port and the ports out of its affected area are not modeled in the PEM. An example is shown in Fig. 6 where the affected area of port $(4,\ 4)$ is set as 3×3.

Accordingly, as each entry J_{mn} in the Jacobi matrix J reflects the dependency between port m and port n, if the dependency between port m and n is omitted, then we have $J_{mn} = 0$. Therefore, matrix J can be quite sparse if we omit enough port dependencies. As for the circuit representation of a PEM, the number of VCCSs can be reduced dramatically when taking the locality property into account.

As a penalty, the simplified PEMs will introduce overestimated IR drops. Considering the superposition principle, when a voltage source is attached at one port in the global network, the voltages at all other ports will be elevated; the omission of port dependencies removes the elevation of voltage level at one port caused by some other ports, and thus the voltage levels are underestimated.

V. EXPERIMENTAL RESULTS

In this section, we first verify the correctness of the proposed hierarchical method in static analysis with industrial benchmarks. Then, the performance in the transient simulation is tested. Finally, the effectiveness of the simplified PEM is presented.

The benchmarks 3-D-μP, 3-D-μPD, and 3-D-TxRx are extracted from real industrial 3-D chip designs [26]. The 3-D-μP and 3-D-μPD are different versions of a 2-tier multiprocessor design and 3-D-TxRx is a hardware cryptography design with three stacked tiers. The other benchmarks are generated using the model introduced in Section II, where $M \times N \times K$ means there are K tiers and each tier contains $M \times N$ P/G nodes. By default, the wire width is 2.5 μm and the space length between two P/G nodes is 10 μm in these benchmarks. All power pads on tier 1 connect to $V_{dd} = 0.8$ V through the package.

The phrase direct full network simulation and word direct in this section mean that the simulation does not use PEMs and regards all the tiers as a whole. We regard it as a baseline in the experiments. Full PEM means that the PEMs used in the experiment consider all port dependencies, while simplified PEM refers to models considering the locality property.

The software HS3-DPG is implemented using C++ language. The simulation platform is CentOS4.8 with 2 Intel Xeon X5680 CPUs @3.33 GHz (12 cores) and 48 GB RAM. A sparse solver CHOLMOD based on Cholesky decomposition and back substitution is used in this brief for PEM extraction and back substitution. The PEMs of different tiers are computed in parallel.

A. Performance of the Hierarchical Static Analysis

In the static IR drop analysis, the performance of HS3-DPG is shown in Table I. With three industrial benchmarks, HS3-DPG can be 2.021×, 1.944×, and 2.953× faster than the direct full network simulation when the number of tiers is 2, 2, and 3, respectively. The accuracy is also well maintained: compared with the direct full network simulation, the maximum absolute errors of our method are 3.97, 4.26, and 4.51 pV, respectively. Besides, the peak memory allocated by HS3-DPG is 0.625×, 0.633×, and 0.882× smaller compared with the direct full simulation. The HS3-DPG can make better use of computing resources to obtain the voltage distributions of 3-D P/G networks more quickly. In addition, HS3-DPG can gain more benefits when the tier number becomes larger [27].

B. Performance of Hierarchical Transient Simulation

In the transient simulation, the complexity of computing PEMs differs greatly in the fixed-time-step case and the variable-time-step case. In the fixed-time-step case, we run the simulation from 1 ns to 10 μs where the time step is set as 0.1 ns. The results are shown in Table II. Results show the speedup of HS3-DPG declines with the increase of simulation time as we expect. In the variable-time-step case, the results are shown in Table III. The max allowed error is set as 1 mV. As the waveforms in benchmark 3-D-μP change rapidly, the time step length is compressed, and thus the actual runtime with

TABLE III
RUNTIME COMPARISON OF THE VARIABLE-TIME-STEP TRANSIENT SIMULATION

Simulation time (ns)		1	5	10	15	30	50
3-D-μP	Direct	18.234s	92.112s	201.341s	309.798s	421.230s	587.122s
	HS3-DPG	11.452s	15.247s	46.186s	60.558s	168.489s	197.174s
	Speedup	1.592	6.041	4.359	5.115	2.500	2.978

TABLE IV
COMPARISON BETWEEN FULL PEM AND SIMPLIFIED PEM

TSV cluster array	Simulation using full PEMs			Simulation using simplified PEMs		
	Sparsity of the Jacobi matrix	Peak Memory (MB)	Max absolute error (V)	Sparsity of the Jacobi matrix	Peak Memory (MB)	Max absolute error (V)
10x10	1.00	694.98	0.80e-12	0.49	658.86	1.50e-4
13x13	1.00	853.83	1.01e-12	0.33	717.58	2.62e-4
20x20	1.00	1847.61	1.00e-12	0.16	862.12	2.24e-4
48x48	0.62	4086.30	1.04e-12	0.032	1093.07	2.72e-4

variable time steps is much longer than that of the fixed-time-step case.

C. Analysis of Simplified PEMs

As mentioned in Section IV, simplified PEMs considering the locality property are expected to reduce memory consumption, while overestimating the IR drops. For a 1000 $\times$ 1000 $\times$3 P/G network, when the simplified PEMs only consider the port dependencies inside the surrounding 4 $\times$ 4 TSV clusters of one port, the results are shown in Table IV. It should be noted that the direct full simulation is regarded as the baseline and all errors with simplified PEMs are negative. Since the Jacobi matrix J of the simplified PEM is significantly sparser than that of the full PEM, the global network using simplified PEMs contains fewer VCCSs and consumes less memory. We also verify that the smaller affected area of one port in the simplified PEM introduces more overestimated IR drops in [27].

VI. CONCLUSION

In this brief, we propose a hierarchical simulation method called HS3-DPG, which is suitable for 3-D P/G network simulation in both static and transient cases. The PEM is introduced to mask the details of the P/G grid in each tier and ensure full parallelism. To further simplify the PEM, we also introduce the locality property into the 3-D P/G network simulation. Experimental results have shown that the hierarchical method can achieve high speedup and maintain the accuracy, while reducing the memory consumption.

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