Exploration of Electrical and Novel Optical Chip-to-Chip Interconnects

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***Abstract*—With the rapid development of parallel computing technologies, there is an urgent demand on increasing the data transmission bandwidth in computer systems. The traditional electrical off-chip interconnect becomes a bottleneck due to the limited number of I/O pins and the limited per-pin-bandwidth. As an alternative, optical interconnect can support tremendous data bandwidth thanks to low transmission loss and wavelength division multiplexing techniques, but suffers from severe power overhead. Recently, optical orbital angular momentum (OAM) has stimulated much interest due to the very high data carrying ability. In this work, we fully evaluate and compare these off-chip interconnect schemes, and propose the novel OAM-based high-bandwidth interconnect structure, which is the most power-efficient.**

***Index Terms*—chip-to-chip interconnect, electrical wire, micro-bump, optical, OAM**

I. Introduction

Since mainstream computer systems are still based on "von Neumann architecture" where computing units and memories are separated, the "memory wall" effect becomes one of the most severe bottlenecks for high-performance parallel computing. With the development of CMOS technology, more and more computing resources can be integrated into a single chip. However, the gap between data computing ability and data transmission ability is continually growing. For example, the recently released graphic card (integrated with two GPUs) by AMD, Radeon R9 295X2, has 5632 stream processors and supports 640GB/s peak bandwidth for off-chip GDDR memory access. The average bandwidth for each stream processor is only 0.11GB/s.

Nowadays, the biggest impediment to improving the performance of exascale computer systems, is the fundamental physical limit of the off-chip electrical interconnect. The total number of I/O pins of a processor is constrained by the packaging, and a large portion of the pins are for the power supply to form a reliable power distribution network (PDN), which limits the number of data pins. For traditional electrical memory connections, the maximum data transmission rate is limited by the physical device layer (PHY), which is about 5-6 Gbps in state-of-art products. The limited pin-count and per-pin-bandwidth restrict the maximum data transmission bandwidth between chips. Recently, fruitful work has been conducted to improve the memory bandwidth through high-density through-silicon-vias (TSVs) by stacking memory directly on the computing cores. Although the data bandwidth can be efficiently increased, the available capacity of stacked memory is limited due to manufacturing and packaging costs. TSV-based 3D stacked memory architecture, therefore, is more appropriate for "smaller scale" embedded systems or low-level caches. Furthermore, the severe heat dissipation and complicated 3D co-design issues are still challenging. Alternatively, the interposer-based 2.5D integration provides a more practical solution than the ideal TSV-based 3D integration due to better heat dissipation, simpler design, and lower manufacturing cost. For example, Xilinx has announced "the biggest FPGA in the world" by integrating four separate Vertex-7 FPGAs on the same interposer. Although the interposer-based 2.5D integration is superior in data bandwidth and power consumption, the per-pin bandwidth is still limited.

Recently, optical communication promises to alleviate many problems posed by off-chip electrical interconnects due to the high speed and low transmission loss. With the traditional on-off modulation, each light beam can only carry one bit of data. Multiplexing methods, such as dense wavelength division multiplexing (DWDM), are utilized to increase the bandwidth. DWDM with existing silicon photonics however has the following issues: 1) a great number of ring resonators with different sizes are required to modulate and receive optical signals for different wavelengths, and each resonator needs an associated tuning heater to compensate the process variations; 2) off-chip or on-chip lasers consume significant power to generate light beams with different wavelengths.

Since the pioneering work proposed by Allen in 1992 [1], orbital angular momentum (OAM)-based optical transmission has stimulated much interest [2], [3] in academia. **OAM of light has the unique characteristic of spiral flow of electromagnetic energy and helical wave-front which provides an additional dimension to carry information**. Allen [1] showed that helically phased light beams comprising an azimuthal phase term $exp(il\varphi)$ have the nature of unlimited number of potential states which means that the OAM of light can ideally carry infinite amount of data. OAM-based optical interconnection, therefore, has the potential to tremendously increase data transmission bandwidth [2], [3] with manageable power overhead. Most previous OAM-related work focuses mainly on the OAM light beam generator and multiplexing techniques in the device level [2], [3], [4], [5], [6]. To implement the OAM-based interconnection in computer systems, the corresponding physical structure and electrical model should be carefully explored, and the advantages and drawbacks

need to be comprehensively evaluated and compared with the traditional electrical and optical interconnects.

In this work, we first present the system structures of four chip-to-chip data transmission mechanisms: the traditional PHY-based electrical interconnect, the interposer-based micro-bump, the traditional fiber-based optical interconnect with DWDM, and the novel OAM-based free space connection. Then, the characteristics of these mechanisms are analyzed. To analyze the OAM-based interconnect, a detailed electrical model in the device level is developed. Finally, the power consumption and bandwidth are fully evaluated and compared for these four mechanisms.

II. Background and System Architecture

For mainstream computing systems, PHY-based electrical wires are still the primary solution for chip-to-chip data transmissions. Interposer-based 2.5D integration, fiber-based traditional optical interconnect, and OAM-based wireless interconnects are potential alternatives. In this section, the system structures of these four chip-to-chip data communication mechanisms are described in detail.

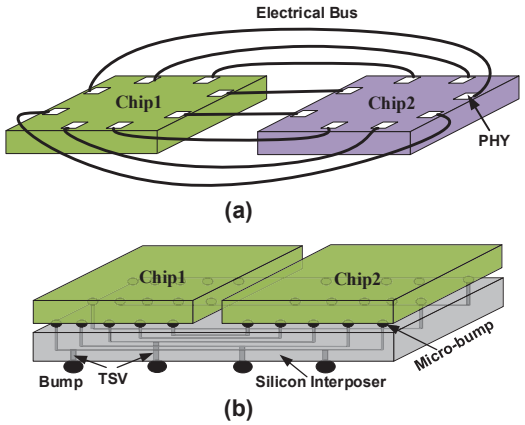

Fig. 1. (a) Diagram of PHY-based electrical wires and (b) diagram of interposer-based 2.5D integration

A. PHY-based Electrical Wires

To meet the high-speed demand of off-chip data communication between memories and processors, special circuits referred to as PHYs are often adopted, which consist of high-speed I/Os, high-resolution delay lock loops (DLLs), and special high-speed control logic. Figure 1 (a) shows the system structure of the traditional PHY-based chip-to-chip interconnects.

B. Interposer-based 2.5D Integration

In the interposer-based 2.5D integration, dies are attached to a passive silicon interposer with micro-bumps. The connection between different dies are implemented with the metal wires on the interposer. Rather than the true 3D integration, TSVs in 2.5D integration are only needed in the interposer to tap out pins, minimizing manufacture and design costs. With features 100-1000x smaller than the package substrate balls, the dense micro-bumps of the interposer-based 2.5D integration can achieve orders of magnitude more connections. The wires between the dies are also much shorter, which can dramatically reduce latency and power consumption. Figure 1 (b) shows the system structure of interposer-based 2.5D integration.

C. Fiber-based Optical with DWDM

The conventional fiber-based optical interconnect for chip-to-chip data communications includes an off-chip laser source, a modulator, an optical fiber, and a photo-diode receiver [7], [8], as shown in Figure 2. Udipi *et al.* proposed to combine memory and a controller with photonics through 3D-stacking, assuming that a single waveguide is capable of providing roughly 80GB/s of bandwidth with 64-wavelength multiplexing [8]. The authors, however, neglected the severe area and power overhead to modulate the light with different wavelengths. This overhead is proportional to the multiplexing depth. Furthermore, the calibration of the wavelength shift in the resonator ring due to process and temperature variations remains a challenge for DWDM.

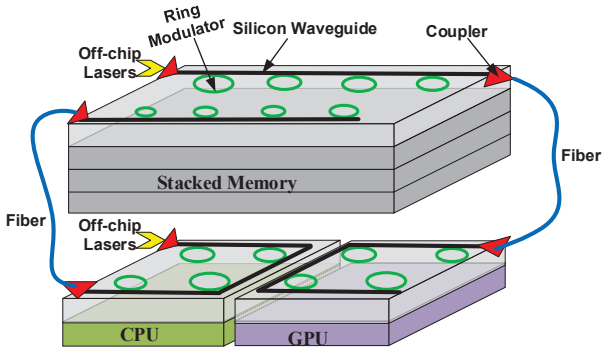

Fig. 2. Diagram of fiber-based traditional chip-to-chip optical interconnect

D. OAM-based Wireless Interconnect

Fruitful work has been conducted to explore the characteristics of OAM beams [2], [3], [4], [5], [6], which has mainly focused on the device. Cai *et al.* reported a silicon-integrated optical vortex emitter to generate well-controlled OAM beams [2]. The smallest device they fabricated has a radius of 3.9 micrometers, which is similar to the radius of a TSV. Their work also shows that the OAM generator has good scalability and is compatible with silicon process for wide-ranging applications. In addition, Wong *et al.* proposed a method for excitation of OAM in helically twisted photonic crystal fiber [5].

Most of the previous work related with OAM beams mainly focused on utilizing them as information carriers for multiplexing [2], [4], [5], [6]. In contrast, Zhang *et al.* proposed an encoding and decoding-based OAM generator for wireless optical communications [3]. The optical OAM can be encoded by modulating the mode order of the ring resonator at a certain wavelength to achieve high data transmission bandwidth, which has better compatibility with the CMOS process with lower overhead.

Figure 3 shows the diagram of OAM encoding/decoding. It mainly consists of a ring resonator, a bus waveguide, and 16 downloading units. Each downloading unit includes an arc waveguide and a grating. The 16 downloading units are distributed equidistantly around the circle and coupled to the ring. If the central frequency of input light injected from the input-port of the bus satisfies the resonance condition of the ring resonator, it will be coupled into the ring and propagates

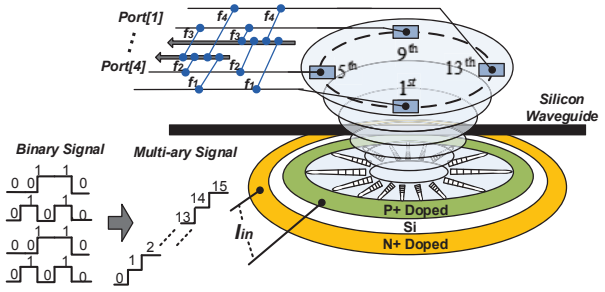

Fig. 3. Diagram of OAM beam generator [3] and the principle of encoding/decoding data with OAM beams

along the ring as whispering-gallery-mode (WGM). Then it will be downloaded by each of the 16 arc waveguides. Finally, the light propagating in all arc waveguides will be combined and transformed into free space light (or travels in homogenous and isotropic mediums) at the end of gratings. Since the phase shift of the propagating light at each downloading unit varies successively, the phase of the output light beam superposed from gratings is azimuthally dependent. In other words, an OAM beam with azimuthal phase dependence of $exp(il\varphi)$ is generated. The orders of OAM beams can be tuned by applying control signals (current or voltage) on the p-i-n junction to modulate the refractive index of silicon [3].

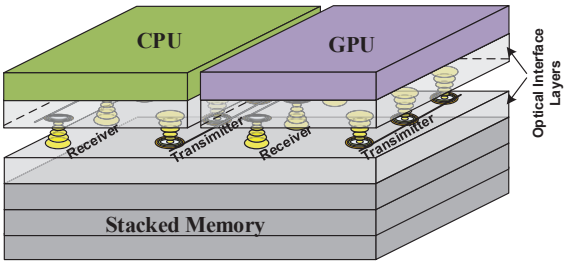

Fig. 4. Diagram of OAM-based wireless chip-to-chip optical interconnect

Figure 4 shows the schematic of OAM beams to be utilized as wireless chip-to-chip optical interconnect. The transmitted binary signals from the processors, such as memory access request and address signal, are converted into the pre-defined multi-ary current signals through a data conversion circuit and applied on the OAM beams generator located on the optical interface layer to produce the tuned OAM beams. The gratings on the optical interface layer located at the destination chip (such as the stacked wide-I/O memory), will receive the lights and recover the original binary signals sent from the processors. When the processors need data from other chips (such as the stacked wide-I/O memory), a similar but reversed optical interconnect can accomplish.

III. A COMPACT MODEL OF OAM-BASED WIRELESS OPTICAL INTERCONNECT

Traditional PHY-based electrical interconnects have been widely implemented in microprocessor products, and interposer-based micro-bumps and fiber-based optical interconnects have also been well studied with prototypes. The novel OAM beam-based interconnect however has not been well analyzed at the system level. To implement the OAM-based wireless optical interconnect in computer systems, a compact model of this interconnect is essential to help the designer reduce design time and evaluate system performance at early design stages. In this section, we develop a compact model for the encoding/decoding-based OAM beam generator.

Figure 5 shows a cross-section view of the p-i-n junction in an OAM generator. The light coupled into the ring resonator propagates as the WGM. Note that N arcs can produce N OAM beams with order from $-N/2+1$ to $N/2$. The relationship between the variation of WGM order $\triangle N_{WGM}$ and OAM order N_{OAM} can be written as:

$$N_{OAM} = \begin{cases} \triangle N_{WGM} & (\triangle N_{WGM} \leq \frac{N}{2}) \\ \triangle N_{WGM} - N & (\triangle N_{WGM} > \frac{N}{2}). \end{cases} \quad (1)$$

When there is no modulation signal applied on the ring, which also means that there is no current injected into the p-i-n junction, the order of WGM for the propagated light can be calculated according to the following formulation

$$N_{WGM} = \frac{L \times Si_{eff}}{\lambda}, \quad (2)$$

where L is the circumference of the ring resonator, Si_{eff} is the equivalent refractive index of silicon in the p-i-n junction, and λ is the wavelength of the light.

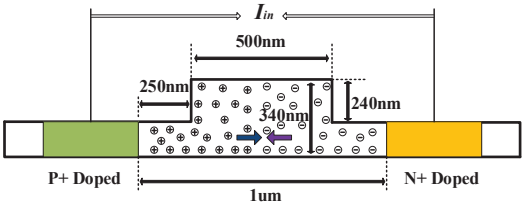

Fig. 5. Cross-section of the p-i-n junction in an OAM generator

When current is injected into the p-i-n junction, which leads to a voltage drop across the p-i-n junction, the variation on the silicon refractive index $\triangle Si_{eff}$ is a function of the variation of the carrier density (electrons and holes) [11]. $\triangle Si_{eff}$ can be described as:

$$\triangle Si_{eff} = -(8.8 \times 10^{-22} \times \triangle n_e + 8.5 \times 10^{-18} \times (\triangle n_p)^{0.8}). \quad (3)$$

The density changes of the electrons ($\triangle n_e$) and holes ($\triangle n_p$) under a certain voltage drop V can be described with the following expressions

$$\triangle n_e = n_{e_o} \times (e^{\frac{q \times V}{kb \times T}} - 1), \quad (4)$$

$$\triangle n_p = n_{p_o} \times (e^{\frac{q \times V}{kb \times T}} - 1), \quad (5)$$

where n_{e_o} and n_{p_o} are the initial density of electrons and holes, respectively. Then, the tuned order of WGM can be obtained as

$$\triangle N_{WGM} = \frac{L \times (Si_{eff} + \triangle Si_{eff})}{\lambda} - N_o. \quad (6)$$

TABLE I
POWER AND PERFORMANCE COMPARISON OF FOUR DIFFERENT CHIP-TO-CHIP INTERCONNECTS.

Interconnects	Package/Chip Size	Size/Pitch @Process	Data Rate	Peak Bandwidth Limited by Area	Total Power	Peak Bandwidth With 100W Power Budget	Normalized Power
PHY-based I/O Pin	Package Size: 5cm X 5cm	Pitch: 1mm @TSMC 28nm	5.5Gbps	1.72TB/s	227W	758GB/s	132mW/(GB/s)
Microbump-based Interposer	Chip Size: 2cm X 2cm	Pitch: 55μm @TSMC 40LP/40G [9]	5.5Gbps	90.9TB/s	520W	17.48TB/s	5.72mW/(GB/s)
Fiber-based Optical		Diameter: 3μm @HP Lab [10]	5Gbps	6900TB/s	10200W	67.6TB/s	1.48mW/(GB/s)
OAM Beams		Diameter: 7.8μm @Bristol Univ. [2]	5Gbps	4100TB/s	5690W	72.1TB/s	1.39mW/(GB/s)

$*Peak\ Bandwidth = \frac{ChipArea}{Pitch^2} \times \frac{DataRate}{8}$; $Power = \frac{ChipArea}{Pitch^2} \times PowerPerUnit$; $NormalizedPower = \frac{Power}{PeakBandwidth}$

As Figure 5 shows, when a current signal is applied to the p-i-n junction, it can lead to charge diffusion for electrons and holes. According to the famous "Einstein Relation", the electron (hole) diffusion length L_e (L_p) is related to the life-time of the electron t_e (t_p) according to expressions (7) and (8), in which D_e, D_p are the diffusion coefficients for electrons and holes, and can be obtained from expressions (9) and (10). μ_e and μ_p are the mobility for electrons and holes, respectively. Based on expressions (7-10), we can calculate the current density J in the p-i-n junction, as shown in (11), in which K_b and T are the Boltzmann constant and Kelvin temperature, respectively. The current through the p-i-n junction, therefore, can be calculated by multiplying the current density J with the area of the p-i-n junction cross-section A according to expression (12).

$$L_e = (D_e \times t_e)^{0.5} \tag{7}$$

$$L_p = (D_p \times t_p)^{0.5} \tag{8}$$

$$D_e = \frac{\mu_e \times K_b \times T}{q} \tag{9}$$

$$D_p = \frac{\mu_p \times K_b \times T}{q} \tag{10}$$

$$J = q \times (\frac{D_e}{L_e} \times n_{e_o} + \frac{D_p}{L_p} \times n_{p_o}) \times (e^{\frac{q \times V}{kb \times T}} - 1) \tag{11}$$

$$I = J \times A \tag{12}$$

$$P = I \times V \tag{13}$$

From expressions (1-12), we can determine the relationship between the applied current I and the tuned order of OAM. Finally, the consumed power to modulate the orders of OAM for each ring can be stated as (13).

IV. PERFORMANCE AND POWER COMPARISON

Based on the four chip-to-chip data transmission mechanisms described in Section II, and the device model of OAM beam generator presented in Section III, the power consumption and data communication bandwidth can be fully compared for these different chip-to-chip interconnects; in particular, the potential of using OAM beams as a novel chip-to-chip interconnects is analyzed in detail.

For the PHY-based traditional electrical wire, the design parameters are from a design with TSMC 28nm technology. The design parameters of the interposer-based micro-bump are from TSMC 40nm technology [9]. The data rate of the PHY is assumed to be 5.5Gbps for both of these

TABLE II
THE ENERGY/POWER PARAMETERS OF FIBER-BASED AND OAM-BASED INTERCONNECT COMPONENTS

Component	Laser	Receiver	Tuning	Ring	DAC
Fiber	0.015 mW/bit	440 uW/bit	250 uW/bit	47fJ/bit	-
OAM				6mW/ring	3.84uW

electrical interconnects. For the fiber-based and OAM-based optical interconnects, the energy/power parameters for each component in these structures are listed in Table II. Since the fiber-based micro-rings with different sizes are more sensitive to process variations due to cross-channel interference, they usually consume more thermal tuning power than the single-sized OAM-based micro-rings. For simplicity, the thermal tuning power for both of these optical interconnects, however, is assumed to be the same. As stated in Section II, unlike the traditional fiber-based optical interconnect, additional data encoding circuit, such as a digital-to-analog converter (DAC), is necessary for the OAM-based interconnect to generate the control signal to modulate the OAM beams. In this work, a 4-bit DAC is utilized to convert the original binary signal into an analog control signal. The power of the DAC is referred to the work by X. Zheng, *et al*. [12]. Although in the fiber-based interconnect with DWDM, the sizes of the micro-rings need to be differentiated for each wavelength, in this work, we also assume all the micro-rings have the same size for simplicity (the reported minimum radius of the micro-ring is 1.5um [10]). Meanwhile, Cai *et al.* reported a silicon-integrated optical vortex emitter with the smallest radius of 3.9 micrometer to generate well-controlled OAM beams [2], which has a similar principle to the approach proposed by Zhang *et al.* [3]. For a fair comparison, the chip sizes for all the four interconnect schemes are assumed to be the same, 2cm×2cm. Note that the PHY-based electrical I/O pins are limited by the package area, we assume the package size is 5cm×5cm for a die size of 2cm×2cm. In order to explore the maximum potential of high-bandwidth, we put as many interconnects as permitted by the die/package area.

The bandwidth and power consumption for the four chip-to-chip interconnects are listed in Table I. The maximum achievable bandwidth due the die/package size limit is shown in column five. Due to the smaller optical features, the optical interconnects have orders of magnitude higher bandwidth than the electrical interconnects. For the electrical interconnects, a significant portion of the chip pins/micro-bumps are utilized for power delivery. The maximum bandwidth of electrical interconnects should be smaller than the values in the ta-

ble, which makes the optical approaches more preferable. The corresponding power for these ideal cases, however, is unrealistically high as shown in column six in Table I. To provide a more practical evaluation, the peak bandwidth under a 100W I/O power budget is listed in column seven for the four schemes. The power consumption per GB/s bandwidth is used to evaluate the power efficiency and is listed in column eight in the table. It can be seen that optical interconnects still outperform electrical interconnects in terms of bandwidth and power efficiency, and the OAM-based approach is the most power efficient. For the fiber-based traditional optical interconnect shown in Figure 2, many couplers and fibers are needed to provide the high data transmission bandwidth (about 1000 couplers to achieve 67.6TB/s), which is still challenging if placing so many couplers peripherally on the chip. The data transmission rate of the OAM-based interconnect is mainly restricted by the performance of the DAC and the OAM orders that the micro-ring can generate. In this work, a conservative assumption is made (4-bit DAC working at 5GHz, and each OAM generator can generate 16 OAM beams with different orders). If a higher speed DAC is employed or one micro-ring can generate more OAM beams with different orders, the power consumption and data transmission bandwidth of the OAM-based interconnect can be further improved. Although novel optical interconnects can provide desirable higher data transmission bandwidth with lower power consumption, the severe cost overhead of stacking an additional optical interface layer on the original die needs to be carefully evaluated.

V. Conclusion

In this work, we present the system structures of four chip-to-chip data transmission mechanisms: the traditional PHY based electrical interconnect, the interposer-based micro-bump, the traditional optical interconnect with DWDM, and the novel OAM-based free space connection. Based on the device model of the OAM beam generator proposed in this work, the power, area, and bandwidth of these four chip-to-chip interconnects are fully analyzed and compared. The proposed OAM-based approach shows the highest power efficiency.

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