Assessment of Circuit Optimization Techniques Under NBTI

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Editor's notes:
This paper conducts a comprehensive study on existing circuit optimization techniques against NBTI, degradation mechanism that has become a critical reliability issue for nano-scaled IC design. These techniques are categorized by their intrinsic characteristics, and several important observations are made to give design guideline on NBTI mitigation.
—Antonio Rubio, UPC

■ **As technology scales,** reliable circuit design to mitigate critical reliability mechanisms (such as negative bias temperature instability (NBTI), hot carrier injection, time-dependent dielectric breakdown, and random telegraph noise) has become a critical challenge for IC designers [1]. Temporal degradation in CMOS transistors or interconnects over the lifetime must be carefully addressed to ensure the chip reliability.

BTI is the major reliability challenge when gate-dielectric thickness becomes thinner than 2 nm [1]. NBTI has attracted great attention in recent years. NBTI increases the threshold voltage of PMOS transistors when they are negatively biased. After a period of operation, circuit delay will exceed the design specification, leading to timing violations and logic failures. Many publications have analyzed the impact of NBTI on circuit performance or provided circuit optimization techniques under NBTI. Some optimization techniques were briefly studied [2]. However, to our knowledge, there is no survey paper that gives a comprehensive summary for NBTI-aware circuit optimization techniques. This paper presents a comprehensive view of the existing optimization techniques under NBTI and explores the generalities of them, to give design guideline on NBTI mitigation. Three observations are made.

1) NBTI-aware circuit optimization techniques can be either compensation techniques or mitigation techniques. The two categories focus on reducing different parts of circuit delay, and they have different efficiency, overheads, and complexity.
2) All the optimization techniques tune electrical parameters which are easy to adjust, such as supply voltage, threshold voltage, and stress time. Reducing stress time is the most efficient method.
3) Leakage reduction techniques can also be used for NBTI mitigation, because both leakage currents and NBTI effects strongly depend on the input states of gates and the gate overdrive.

The rest of this article is organized as follows. Background introduces the background about the NBTI physics and NBTI modeling. Circuit optimization techniques under NBTI summarizes the NBTI-aware circuit optimization techniques. Finally, Comparison and conclusions compares all the mentioned techniques and concludes the article.

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Background

This section briefly introduces the NBTI physics, the NBTI models, and the impact of NBTI on the CMOS gate delay.

NBTI physics

A popular physical origin of NBTI is the reaction-diffusion (R-D) mechanism [3], where NBTI is described as the generation of charges in the Si/oxide interface. When a PMOS transistor is negatively biased (stress), some holes in the inversion layer interact with the Si-H bonds in the interface. These Si-H bonds can be easily broken by hole capture under the electrical stress at elevated temperature. The broken Si bonds act as interface traps and consequently, the threshold voltage increases. The dissociative H atoms can diffuse away from the interface toward the gate or anneal the existing traps (recovery).

NBTI can be alternatively explained by the trapping-detrapping (T-D) mechanism [4], where defects in the gate dielectrics can capture carriers, causing the threshold voltage to degrade; when the captured carriers are emitted back, the threshold voltage is recovered. It is summarized that the R-D mechanism is inconsistent with some measured data, and the T-D mechanism is able to explain the bulk of the data [4]. But the T-D model still cannot explain the permanent (unrecoverable) component of NBTI. The physical explanation of NBTI is still under investigation by the device research community.

NBTI model

Take the R-D model as example, NBTI has two states: stress and recovery. To predict the long term threshold voltage degradation (ΔV_{th}) due to alternate stress and recovery phases, a closed form for the upper bound of ΔV_{th} is proposed [5]

$$\Delta V_{th}(t) = \left(\frac{\sqrt{K_v^2 T_{clk}\omega}}{1-\beta_t^{1/2n}}\right)^{2n}$$
$$\beta_t = 1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(1-\omega)T_{clk}}}{2t_{ox}+\sqrt{Ct}}$$
$$K_v = \left(\frac{qt_{ox}}{\varepsilon_{ox}}\right)^3 K^2 \frac{\varepsilon_{ox}}{t_{ox}}(V_{gs}-V_{th})\sqrt{C}\exp\left(\frac{2E_{ox}}{E_0}\right) \quad (1)$$

where t_{ox} is the oxide thickness; $\varepsilon_{ox} = 3.453133 \times 10^{-11}$ F/m; $E_{ox} = (V_{gs} - V_{th})/t_{ox}$; $C = \exp(-E_a/(kT))/T_0$, $T_0 = 10^{-8}$; E_a, E_0 and K are obtained by fitting measured data; T_{clk} is the time period of one stress-recovery cycle; ω is the duty cycle (the ratio of time spent in stress to time period); ξ_1 and ξ_2 are two constants; $n = 1/6$ for a H_2 diffusion model, and for a H based model $n = 1/4$; t_e either equals t_{ox} or the diffusion distance of hydrogen in the initial stage of recovery.

Based on (1), ΔV_{th} strongly depends on the overdrive ($V_{gs} - V_{th}$) and ω, as shown in Figure 1.

Gate delay model

Gate delay under NBTI is expressed as

$$D(t) = D_{intr} + \Delta D_{NBTI}(t) \quad (2)$$

where D_{intr} is the intrinsic delay without considering NBTI, and $\Delta D_{NBTI}(t)$ is the NBTI-induced delay shift at time t.

D_{intr} is expressed as

$$D_{intr} = \frac{KC_L V_{dd}}{A(V_{dd} - V_{th0})^{\alpha}} \quad (3)$$

where K is a physical constant, A is the area of the device, C_L is the load capacitance, and α is the velocity saturation index ($1 < \alpha < 2$).

$\Delta D_{NBTI}(t)$ is expressed as

$$\Delta D_{NBTI}(t) \approx \frac{\alpha \Delta V_{th}(t)}{V_{dd} - V_{th0}} \times D_{intr}. \quad (4)$$

D_{intr} and $\Delta D_{NBTI}(t)$ both strongly depend on V_{dd} and V_{th0}, as shown in Figure 2.

Circuit optimization techniques under NBTI

This section summarizes the existing circuit optimization techniques under NBTI. They are categorized by analyzing the parameters in the above models. Based on (2), to decrease gate delay under NBTI, one can decrease either D_{intr} or $\Delta D_{NBTI}(t)$. For the former, the intrinsic delay is decreased to leave larger time margin for NBTI degradation, it is therefore a compensation method. The latter is an actual NBTI mitigation method. Note that when reducing one of D_{intr} and $\Delta D_{NBTI}(t)$, the other may be affected.

NBTI compensation techniques

NBTI compensation is to decrease the intrinsic delay, such that delay under NBTI still satisfies the design specification. Based on (3), three parameters can be tuned to decrease D_{intr}: A (device area), V_{dd}, and V_{th}.

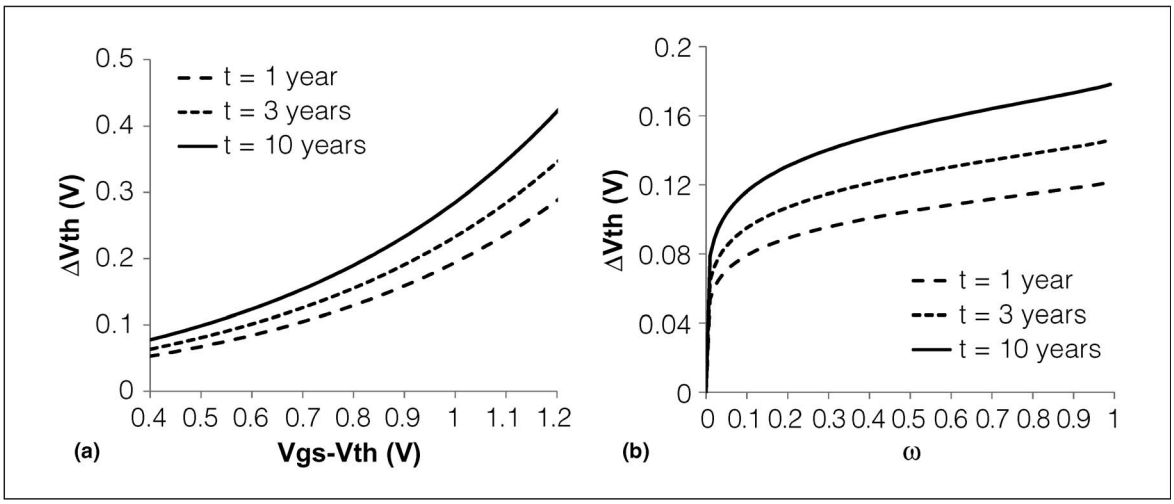

Figure 1. Results of (1): dependence of NBTI on the overdrive voltage and the duty cycle. The model parameters are obtained from [5], $t_{ox} = 1.2$ nm, $T_{clk} = 0.01$ s, $T = 378$ K, $n = 1/6$, $V_{th} = 0.5$ V. (a) Dependence of NBTI on $V_{gs} - V_{th}$. $\omega = 0.5$. (b) Dependence of NBTI on ω. $V_{gs} = 1.2$ V.

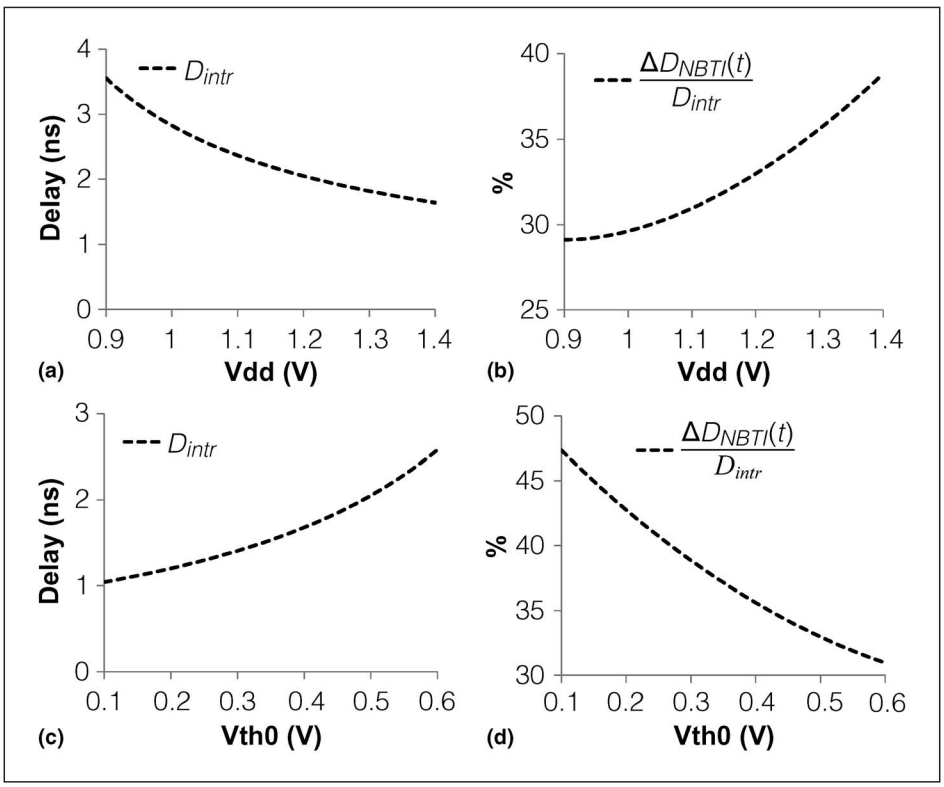

Figure 2. Results of (3) and (4): dependence of the intrinsic delay and NBTI-induced delay degradation on V_{dd} and V_{th0}. $KC_L/A = 1$ ns, $\alpha = 1.5$, $t = 10$ years, $\omega = 0.5$, the NBTI model parameters are same as those used in Figure 1. (a) Dependence of the intrinsic delay on V_{dd}. $V_{th0} = 0.5$ V. (b) Dependence of NBTI-induced delay degradation rate on V_{dd}. $V_{th0} = 0.5$ V. (c) Dependence of the intrinsic delay on V_{th0}. $V_{dd} = 1.2$ V. (d) Dependence of NBTI-induced delay degradation rate on V_{th0}. $V_{dd} = 1.2$ V.

Tuning device area. Larger transistor leads to smaller intrinsic delay by introducing some area penalty. Paul et al. studied gate-level sizing [6], which was formulated by the following equation:

$$\begin{aligned} &\text{minimize} \sum_{i=1}^{N} \alpha_i x_i \\ &\text{subject to} \\ &\sum_{i \in p} D_i \le A_0 \qquad \forall p \in P \\ &L_i \le x_i \le U_i \qquad i = 1, \cdots, N \end{aligned} \tag{5}$$

where x_i is the size of gate i, α_i is the weight for gate i, L_i and U_i are the lower bound and upper bound of x_i, D_i is the delay of gate i in the path p, and N is the number of gates in the circuit. In short, (5) is to minimize the total area such that the NBTI-aware circuit delay satisfies A_0. With an average of 8.7% area overhead, gate sizing can ensure reliable performance for 10 years [6].

Kang et al. studied a finer-grained transistor-level sizing method [7], in which the pull-up and pull-down networks in the same gate could be sized to different ratios. This method reduces the area penalty of gate-level sizing by an average of 43%. Khan et al. studied another transistor-level sizing method that considered the impact of transistor sizing on its adjacent gates [8]. It further reduces the area overhead by 50% as compared with [7].

Tuning V_{dd}. As shown in Figure 2(a) and (b), higher V_{dd} significantly decreases D_{intr} but NBTI degradation will be faster. A static implementation of V_{dd} tuning is guard-banding, which gives circuit a high protection strength, leading to large positive slacks during early time and large power overheads. With higher V_{dd}, processor can finish its computation faster. As a result, processor can be periodically power gated such that NBTI recovery and power saving are achieved [9]. But this method still has significant area and power overheads (both are larger than 20%).

Most of the V_{dd} tuning methods are dynamic techniques. They adjust V_{dd} when circuit is working, based on dynamically tracked data or pre-scheduled schemes. Chen et al. studied a dual-V_{dd} (high and low) assignment scheme [10]. During circuit operation, once circuit delay exceeds the constraint, high V_{dd} on critical paths is increased to decrease the intrinsic delay (Figure 3). At the same time, low V_{dd} on noncritical gates are decreased for power reduction. This method saves on average 50% leakage as compared to guard-banding, while the NBTI-induced degradation is reduced by 62%.

Some other similar approaches were also studied. A scheduled voltage scaling approach to compensate for NBTI was proposed [11]. In addition to the supply voltage, the bias voltage is also dynamically tuned [12]. A fine-grained self-tuning dynamic voltage and frequency scaling (DVFS) strategy was proposed to maximize the lifetime computational power efficiency [13].

Tuning V_{th}. In a conventional dual threshold voltage assignment (DTVA) approach for leakage reduction, noncritical gates are assigned to high V_{th}, leading to higher intrinsic delay and less time margin. Tu et al. took NBTI into account when performing DTVA for leakage reduction [14]. Circuit lifetime is maintained by assigning more low-V_{th} gates to decrease the intrinsic delay and leaving sufficient margin for NBTI degradation, while leakage is still reduced by assigning high-V_{th} gates.

Kumar et al. studied an adaptive V_{th} tuning method [12]. It dynamically adjusts V_{dd} and V_{th} to decrease the intrinsic delay to compensate for NBTI-induced delay degradation.

High level synthesis (HLS). Kumar also studied an NBTI-aware HLS technique [15]. It maps a circuit to a gate library that considers impact of signal probability on NBTI, to ensure the optimal performance during the entire lifetime. Compared with worse-case synthesis, it method saves 10% area and 12% power.

Summary of compensation techniques. NBTI compensation techniques tune device area, V_{dd} or V_{th} to decrease the intrinsic delay, leaving larger time margin for NBTI degradation. Among the above techniques, simple guard-banding techniques have large positive slack and larger-than-necessary overheads. Adaptive tuning methods have better performance and smaller overheads, but they are complex to implement. Although compensation techniques focus on the intrinsic delay, the NBTI-induced delay shift may be affected or even increased, which should be considered in compensation techniques.

NBTI mitigation techniques

Different from compensation techniques, NBTI mitigation techniques focus on reducing ΔD_{NBTI}. But D_{intr} may be increased due to mitigation techniques, therefore, these methods are usually workload-aware or implemented in standby mode. From (1), three parameters can be tuned to mitigate NBTI: ω(duty cycle), V_{gs}, and V_{th}.

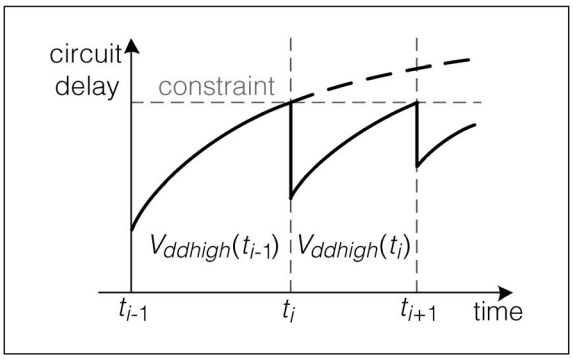

Figure 3. Supply voltage assignment.

Tuning V_{gs}. When V_{gs} is biased to high voltage, $V_{gs} \approx V_{dd}$, so tuning V_{gs} is equivalent to tuning V_{dd}. An on-line dynamic voltage scaling (DVS) scheme was studied [16]. It is based on the observation that lower V_{dd} provides lower NBTI degradation rate (Figure 2b), but with lower V_{dd}, D_{intr} will increase. In this method, V_{dd} is decreased to mitigate NBTI but system performance is still guaranteed according to dynamically tracked timing slacks. It achieves 18% lifetime improvement with 57% power reduction.

Different from the V_{dd} tuning methods belonging to NBTI compensation techniques, this method uses lower V_{dd} to decrease the NBTI degradation rate and therefore belongs to NBTI mitigation techniques.

Tuning V_{th}. From Figure 2c and d, although higher V_{th} leads to larger intrinsic delay, NBTI degradation will be slower. This theory can be used for NBTI mitigation in standby mode. However we do not see any publication that adopts this method.

Tuning the duty cycle. Decreasing the duty cycle is equivalent to reducing the total stress time of PMOS transistors. Since NBTI degradation accumulates with stress time, reducing stress time can greatly mitigate NBTI. There are a variety of techniques that belong to this category.

Input Vector Control (IVC): If stress can be removed, PMOS transistors will undergo the recovery state and consequently, NBTI is mitigated. When circuit is standby, an optimal input vector (IV) is assigned to circuit to obtain a lowest NBTI degradation rate [17], [18]. Since one IV always degrades the same transistors, multiple IVs are alternatively used during the idle periods [19], such that the maximum degradation of any PMOS is reduced. IVC can reduce about 20% $\sim$ 30% of NBTI degradation.

Internal Node Control (INC): To overcome the shortage that IVC cannot control gates with deep logic depth, some INC techniques are proposed: gate replacement (GR) [20], gate modification (GM) [21], and transmission gate insertion (TGI) [22], as shown in Figure 4.

The GR technique replaces a gate $G(x)$ with another library gate $G'(x, sleep)$, such that: when circuit is active ($sleep = 0$), $G'(x, 0) = G(x)$; when circuit is standby ($sleep = 1$), $G'(x, 1)$ can serve as a control point to mitigate NBTI degradation. As illustrated in Figure 4a, when gate G_1 is replaced by G'_1 on the critical path, the stress of G_2 is removed when circuit is standby. In active mode, the logic correctness is not affected.

As illustrated in Figure 4b, in the GM technique, an arbitrary gate is modified by adding two transistors which are controlled by the sleep signal, such that the output of the gate can be forced to any logic value to perform INC. Compared with GR, GM is more general, since for GR, only certain output values can be forced. But GM does not fit the standard cell library based design flow of digital circuits; while for GR, the standard design flow can be directly used.

For TGI, it adds an transmission gate (TG) and a dissociative PMOS transistor to perform INC, as shown in Figure 4c. Compared with GR and GM, TGI has a higher flexibility, and the delay increase caused by the inserted TGs is independent of gate type.

INC techniques can mitigate about 30% $\sim$ 50% of NBTI degradation, which is more efficient than IVC. INC increases the intrinsic delay since extra transistors are added, which also lead to power and area overheads (about 10% $\sim$ 20%). These overheads should be carefully controlled.

Power Gating (PG): PG techniques which are widely used for leakage reduction can be also used for NBTI mitigation. Due to the additional sleep transistors, PG introduces some delay and area overheads, as well as the wake-up time overhead.

Calimera et al. studied the efficiency of PG on mitigating NBTI [23]. The sleep transistor size is carefully decided to achieve the best tradeoff between leakage reduction and lifetime extension. With 2.5% delay and 18% area overheads, circuit lifetime is extended by on average 2×, while leakage is reduced by 91%. They also studied full, partial and clustered PG [24], as shown in Figure 5. Partial PG is only applied to the non-critical paths to obtain a zero delay overhead, and therefore has no benefit for NBTI mitigation. For clustered PG, the non-critical cluster does not affect circuit delay and therefore can tolerate a smaller sleep transistor; while the critical cluster should use a larger sleep transistor. The clustered PG scheme has the best performance among the three schemes. They also studied a partitioned memory approach [25]. Based on the locality of access patterns, some memory subblocks are idle for an amount of time and turned into a low power state to reduce power and mitigate NBTI simultaneously. The lifetime improvement can be up to 2×.

An improved PG scheme for NBTI mitigation was proposed [26]. It consists of several auxiliary sleep transistors with different sizes, which are dynamically configured to different strength based on dynamically tracked data, resulting in 8% ~ 10% more leakage saving than fixed-size PG methods.

Degradation Rates Balancing (DRB): Some techniques try to balance the idle time over all the modules in a system when the system is running, such that the lifetime of the entire system can be maximized. A dynamic re-indexing scheme for cache was proposed [27], where the indexing function was changed over time in order to uniformly distribute the idle time over all the cache lines. The lifetime extension can be up to 3×. A Bit flipping technique was proposed to make signal probability close to 50% to recover the static noise margin (SNM) degradation caused by NBTI for SRAM cells [28]. The SNM is recovered by 30%.

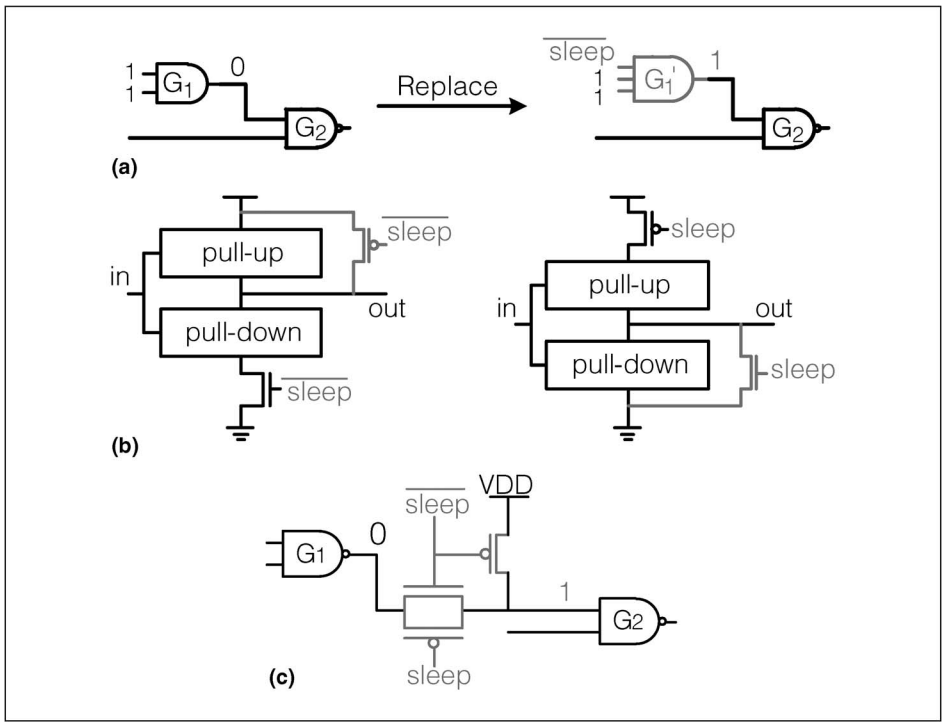

Figure 4. Internal node control. (a) Gate replacement. (b) Gate modification. (c) Transmission gate insertion.

Logic Restructuring (LR)/Pin Reordering (PR): PR is based on the stacking effect in the pull-up network of CMOS gates. PMOS transistors with higher 0 probability should be placed far from power supplies to avoid long-time stress. LR is based on functional symmetries. Symmetric wires can be swapped to reduce the 0 probability to mitigate NBTI. A pure PR technique was studied by Kiamehr et al. [29]. Wu et al. studied a joint LR and PR technique [30], which mitigated NBTI by 56% and had nearly zero overheads.

Summary of mitigation techniques. NBTI mitigation techniques tune V_{dd}, V_{th}, or reduce stress time to mitigate the NBTI-induced degradation. Most of them focus on reducing the stress time of PMOS transistors, because NBTI degradation accumulates with the stress time. NBTI mitigation techniques are usually implemented in standby mode, since internal states are useless in standby mode and can be changed to mitigate NBTI. Since NBTI and leakage both strongly depend on the input states of gates and the gate overdrive, some leakage reduction techniques (e.g., IVC, INC and PG) can be used for NBTI mitigation. NBTI mitigation techniques usually have attractive effects, but they are complex to implement and some methods need to significantly change the physical design of the chip.

Reliability has become a critical challenge for nano-scaled IC design. Design and test solutions at the current technology node and beyond are needed to resolve these reliability issues. This paper focuses on NBTI which is a serious reliability concern, and

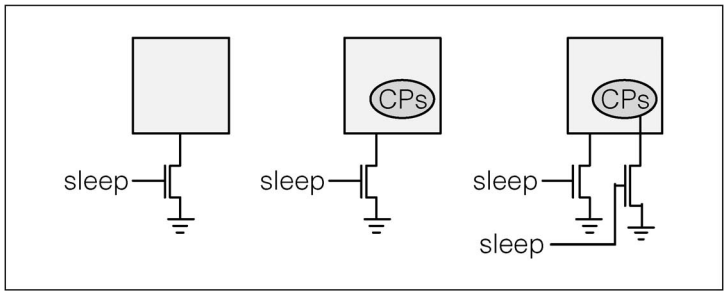

Figure 5. Full (left), partial (middle), and clustered (right) power gating.

Table 1 Summary of NBTI-aware circuit optimization techniques.

Category	Technique	Efficiency	Overhead	Complexity
Compensation	Guard-banding	Low	High	Low
	Gate/transistor-sizing [6-8]	Low	Medium	Low
	Adaptive V_{dd}/V_{th} scaling [9-13]	Medium	Low	High
	Dual threshold voltage assignment (DTVA) [14]	Low	Low	Low
	High level synthesis (HLS) [15]	Medium	Medium	Medium
	Timing slack aware dynamic V_{dd} scaling [16]	Low	Low	High
Mitigation	Input vector control (IVC) [17-19]	Medium	Low	Medium
	Internal node control (INC) [20-22]	High	Medium-high	High
	Power gating (PG) [23-26]	Highest	Medium	Medium
	Degradation rates balancing (DRB) [27,28]	Medium-high	Medium	High
	Logic restructuring (LR)/pin reordering (PR) [29,30]	Medium-high	Almost none	Low

summarizes the existing circuit optimization techniques against NBTI. All the mentioned techniques are briefly summarized in Table 1. Among the compensation techniques, guard-banding, sizing, DTVA and HLS are "one-time" fixed solutions, they add appropriate guard-bands to ensure circuit performance during the entire life, leading to large positive slack during early time and big area/power overheads. Adaptive V_{dd}/V_{th} approaches make circuit delay exactly meet the constraint during the entire life, so the power overhead is much smaller, but they are more complex to implement. Among the mitigation techniques, LR/PR is also an "one-time" fixed solution, but its overhead can be ignored. IVC, INC, and PG are implemented in standby mode, they have no benefit when circuit is active. INC and PG even introduce some delay overhead in active mode. Dynamic V_{dd} scaling and DRB methods are implemented at run-time. The efficiency of DRB can be high, but it is very complex. PG has the highest efficiency among all the techniques. Generally speaking, mitigation techniques have better efficiency than compensation techniques, but mitigation techniques are more complex to implement.

We further make the following conclusions in this paper.

1) NBTI-aware circuit optimization can be implemented by compensation or mitigation. The former decreases the intrinsic delay and the latter decreases the NBTI-induced delay shift. When decreasing one of them, the other may be also affected.
2) All these techniques tune the electrical parameters which are very easy to adjust, such as the device area, V_{dd}, V_{th}, and stress time. When tuning V_{dd} or V_{th}, the intrinsic delay and NBTI-induced delay shift are contradictory, so V_{dd}/V_{th} tuning often has low efficiency or large overheads. Since NBTI degradation accumulates with the stress time, reducing stress time can greatly mitigate NBTI. Consequently, reducing stress time is the most efficient method for NBTI mitigation.
3) Many NBTI mitigation techniques are borrowed from leakage reduction techniques. The reason is that both NBTI effects and leakage currents strongly depend on the input states of transistors/gates and the gate overdrive, though leakage and NBTI have different dependence on the input states [17]. Leakage and NBTI can be mitigated simultaneously, because circuit delay only depends on critical and near-critical paths, these paths can be optimized for NBTI and other paths can be optimized for leakage. This method will decrease the timing slack of noncritical paths and increase the number of critical paths.

Although there are so many circuit optimization techniques against NBTI, the problem is not

completely solved. Techniques with higher efficiency usually have higher overheads or implementation complexity. Consequently, techniques with high efficiency and lower overheads are still needed. In addition, most of the stress reduction techniques are implemented in standby mode, run-time techniques only include adaptive tuning and degradation rate balancing approaches, which are very complex to implement. As a result, low-cost run-time optimization techniques are also required.

Acknowledgment

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