

HS3DPG: Hierarchical Simulation for 3D P/G Network

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Abstract—As different chips are stacked together in 3D ICs, the power/ground (P/G) network simulation becomes more challenging than that of 2D cases. In this paper, we propose a hierarchical simulation method suitable for 3D P/G network (HS3DPG), which can ensure full parallelism and good scalability with the number of tiers. In the IR drop analysis, when there are 9 tiers, the hierarchical method can be 6.5 times faster than the direct full network simulation. The accuracy of HS3DPG has been verified by a 3D P/G network from the industrial design. Besides, we introduce the “locality” property into HS3DPG to further simplify the simulation. Finally, HS3DPG is used to analyze the voltage distribution of a 3D P/G network with clustered TSVs.

Index Terms—3D P/G network; hierarchical simulation; port equivalent model

I. INTRODUCTION

With the feature size shrinking, traditional electronic design methodologies face some bottlenecks, such as per wafer cost, large interconnect delay, and high leakage power. Three-dimensional (3D) integration has been regarded as a promising solution to mitigate these problems mentioned above [1]–[3]. Compared with the traditional 2D integration, the 3D technology can offer many benefits such as the reduction in interconnect wire length, improved memory bandwidth, the support for realization of heterogeneous integration and smaller form factor [4].

As the technology advances, P/G networks have become more and more critical in the chip design flow. Power supply levels may have significant effects on the circuit performance such as power consumption and signal delay. However, the analysis of P/G networks is a very computationally challenging task. There may exist millions of P/G nodes in chips nowadays. The computation is usually extremely time and resource consuming.

Considering the complexity of P/G networks, many researchers have studied the simulation problem in 2D chips. Some multigrid based approaches such as preconditioned conjugate gradient method (AMG-PCG) [5], hybrid multigrid (HMD) [6] and multigrid-like techniques [7] are proposed to accelerate the P/G network simulation. In [8], Zhao *et al* presented a hierarchical analysis approach for 2D P/G networks. This paper uses macromodels to overcome the simulation challenges.

In the power delivery system of 3D chips, the situation of P/G issues will become much tougher than that of 2D cases [9]. P/G TSVs play the role of vertical connections and stack the networks of all chips as a whole. The power coupling between different chips becomes tight and the network scale may be several times larger than that of 2D cases, which is a key problem for the simulation in 3D P/G network. It is necessary to study approaches suitable for 3D P/G network simulation.

There are only a few studies focusing on the modeling and fast analysis of 3D P/G network. Most of them tended to regard the 3D power system as a whole. Huang *et al* [10] extended the theory

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of compact physical model to be applicable to 3D P/G networks in the pre-PD (physical design) validation. Yu *et al* [11] described the electrical-RLC models extracted from 3D P/G networks as state equations. To reduce the simulation complexity of the system, the authors used model order reduction (MOR) methods to compress the scale of matrices in the frequency domain [11].

In both [10] and [11], the number of unknowns in modified nodal analysis (MNA) based equations is the number of total P/G nodes in all tiers, which is huge and difficult to solve. Such methods can not ensure good scalability when the number of tiers increases. Hu *et al* proposed a power distribution network analysis flow to address power delivery issues in 3D chips [12]. They suggested using standard reduced power models (SRPM) to replace some tiers of 3D P/G network. SRPMs can also help 3D chip designers to mitigate the conflict between data sharing and chip protection. However, the key issue is how to build SRPM for each tier.

In this paper, we present a hierarchical simulation method suitable for 3D P/G network: HS3DPG. The proposed method separates all tiers by removing TSVs directly and then extracts the port equivalent model of each tier. After that, the removed TSVs are put back again to connect the port equivalent models together. The final circuits with port equivalent models have much fewer nodes than the original one, which becomes easy to solve. Port equivalent models of each tier are computed in full parallel, so the scalability can be ensured. Besides, by extending the “locality” effect in 2D flip chips [13] to the 3D P/G network, we can further simplify the equivalent model. The hierarchical approach with simplified models occupies much smaller memory when the number of ports becomes large. In the last of this paper, we use HS3DPG to analyze the voltage distribution in a 3D P/G network. Based on the obtained voltage distribution maps, some primary characteristics of clustered TSVs are presented.

The main contributions of this paper are as follows:

- 1) We implement a hierarchical simulation flow for 3D P/G network and use a 3D chip from industrial design to verify the accuracy. Compared with the prior work on the simulation of 3D P/G network, the proposed method can deal with each tier separately.
- 2) We propose a port equivalent model suitable for 3D P/G network, which masks the details of the P/G grid in each tier. It can also be used to solve the conflict between data sharing and chip protection for 3D IC design when using chips from different vendors [12].
- 3) We introduce the “locality” effect into the simulation of 3D P/G network for the first time. Considering the “locality” effect, we can simplify the port equivalent models further, which in turn reduce the complexity of the hierarchical simulation.

The rest of this paper is organized as follows. Section II gives a brief overview of 3D power delivery system. Section III illustrates our hierarchical simulation approach in detail. The “locality” property is introduced to further simplify the hierarchical simulation in Section IV. Experimental results are shown and analyzed in Section V. Section VI concludes the paper.

II. 3D POWER DELIVERY SYSTEM

A. 3D P/G network

A 3D power delivery system with 4 tiers is illustrated in Figure 1. P/G TSVs tunnel through the substrate of each tier to connect the P/G grids as a whole. The P/G network in each tier is usually a mesh-based network as shown on the right part. It is obvious that 3D power delivery system has an inherent hierarchical structure.

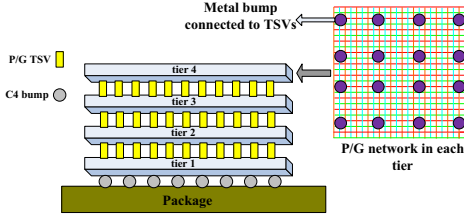


Fig. 1. 3D power delivery system.

Figure 2 shows the detailed metal layers of the P/G network and the full circuit representation of a power network with 4 nodes. In IR-drop analysis, capacitors and inductors in the figure will be ignored. So the on-chip P/G network is extracted as a resistive network in this paper. The TSV is simply modeled as a resistor here. We determine on-chip parameters and wire segment dimensions through PTM(Predictive Technology Model) interconnect models under 45nm technology [14].

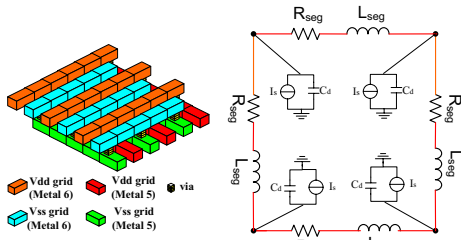


Fig. 2. Circuit extraction of the P/G network.

B. TSV topology

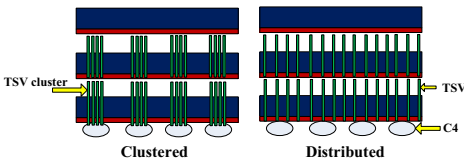


Fig. 3. TSV topology.

In a 3D power delivery system, TSVs perform the role of C4 bumps in intermediate tiers. Figure 3 shows the two ways of TSV locations in 3D P/G network [15]. In the clustered P/G TSV location, several TSVs are clustered together while aligned to C4 bumps in the bottommost tier. In the distributed location, TSVs are distributed over the flat individually. Compared with the distributed P/G TSV location, the clustered one can leave more continuous white space to logic circuits. Besides, a TSV will lead to large unusable white space surrounding it to ensure the manufacturability, which means distributing TSVs individually over the flat is not very practical. In addition, clustered TSVs have higher reliability when one or more TSVs in the system break down. A notable feature of the clustered TSV location is the port number between different tiers is limited, which makes it very suitable for our hierarchical simulation method.

For simplicity, we assume each tier contains the same number of TSV clusters in this paper. But our method can also adapt to the situation in which each tier has the different number of TSV clusters.

III. HIERARCHIAL SIMULATION FOR 3D P/G NETWORK

In consideration of the hierarchical structure of 3D power delivery system, we propose a hierarchical simulation approach for 3D P/G network (HS3DPG) in this section. Subsection A presents a brief overview of the P/G network analysis. After that, subsection B will explain our hierarchical simulation approach in detail.

A. An Overview of the P/G network Analysis

In the IR drop analysis, the P/G network can be modeled as a linear resistive system. The power system with N nodes can be formulated as linear equations by using the MNA method. Besides, if we are only interested in the voltage values, the system can be further reformulated as a symmetric and positive definite (SPD) matrix [7]:

$$Gx = I$$

where $G \in R^{N \times N}$ is a sparse and SPD conductance matrix. $x \in R^{N \times 1}$ is the voltage vector of grid nodes to be computed. $I \in R^{N \times 1}$ is a current vector related to current sources connected to P/G nodes. We choose a sparse Cholesky solver (CHOLMOD [16]) to compute all the SPD matrices in this paper.

B. Proposed hierarchical method with port equivalent models

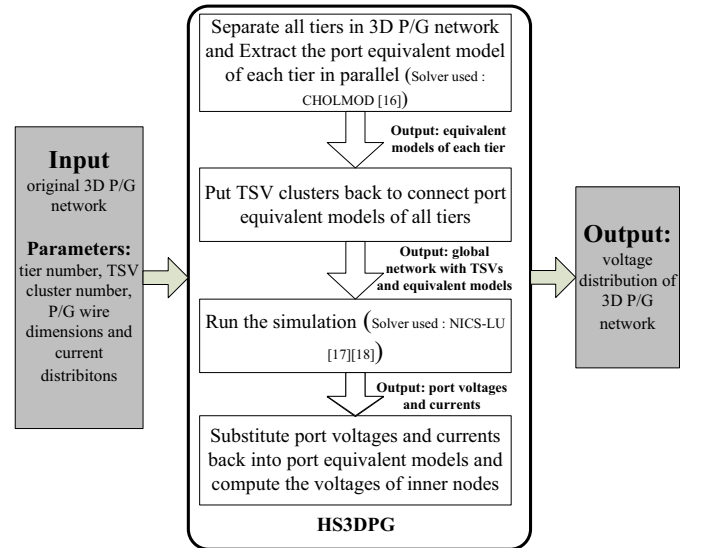


Fig. 4. Simulation flow of HS3DPG.

As mentioned in Section II.A, the 3D power delivery system has a hierarchical structure. The main difference from the 2D P/G network is the existence of P/G TSVs. If we can remove the influence of TSVs, the situation will become easy to solve. That is the starting point of our hierarchical approach. In order to deal with each tier separately, a port equivalent model is proposed in this paper.

In the hierarchical simulation flow shown in Figure 4, we firstly remove all the TSV clusters directly to divide the global network into several independent networks. Then for all tiers, we extract the port equivalent model in parallel and use them to replace the detailed grids of each tier. After that, TSV clusters are put back and connect all the port equivalent models as a new global network. The final network with equivalent models is small that we can run the simulation using

some traditional tools (we choose a recently released NICS-LU [17], [18] solver to compute the final network in this paper). Finally, we substitute port voltages and currents back into the port equivalent model and compute the voltages of inner nodes in each tier.

The key component in HS3DPG is the port equivalent model. We will explain it in detail in the following part.

For one tier, ports are defined as the nodes connected to TSV clusters. In general, one TSV cluster is connected to the metal layer through a C4 bump, which can be regarded as a super node. So the port number of each tier is equal to the TSV cluster number. The proposed port equivalent model of one tier can be formulated as follows:

$$I = J * V + S = \begin{bmatrix} \frac{\partial I_1}{\partial V_1} & \cdots & \frac{\partial I_1}{\partial V_M} \\ \vdots & \ddots & \vdots \\ \frac{\partial I_M}{\partial V_1} & \cdots & \frac{\partial I_M}{\partial V_M} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_M \end{bmatrix} + \begin{bmatrix} S_1 \\ \vdots \\ S_M \end{bmatrix}$$

The port equivalent model used here is similar to the multilevel Newton algorithm with macromodeling in nonlinear circuit analysis [19]. The definitions of I and V are shown in Figure 5. Assuming there are M ports in the current tier, $I \in R^{M \times 1}$ is a current vector flowing into this tier through these ports connected to TSV clusters. $J \in R^{M \times M}$ is a Jacobi matrix reflecting port dependencies, which is different from the macromodel used in [8]. The Jacobi matrix has more explicit physical information about these port dependencies, which can help us use the location information of TSV clusters to simplify the equivalent models later. $S \in R^{M \times 1}$ is a current vector related to current sources attached to P/G nodes in this tier.

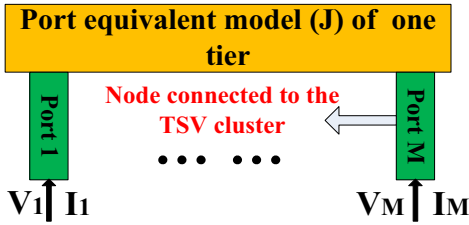


Fig. 5. Port equivalent model of one tier.

We take 2 ports for example to show how to compute the port equivalent model. Two ports means the current tier connect with other tiers through two TSV clusters. The procedure computing S and J can be described in following steps:

- Separate the tier to be computed from the global network by removing the TSV clusters connected to it. For the P/G network in the current tier, write the MNA-based equations:

$$Gx = I$$

The established equations will be used to calculate current vectors needed in the following steps.

- Attach all ports to the ground ($V_1=V_2=0$) and then calculate the current vector flowing into this tier through these two ports. The result is vector S .
- Attach a unit voltage source to port 1 and keep the others connected to the ground ($V_1=1, V_2=0$). Calculate the current vector flowing into this tier through these two ports and then minus vector S . The result is one column of J :

$$\begin{bmatrix} J_{11} \\ J_{21} \end{bmatrix} = \begin{bmatrix} \frac{\partial I_1}{\partial V_1} \\ \frac{\partial I_2}{\partial V_1} \end{bmatrix}$$

- Attach a unit voltage source to port 2 and keep the others connected to the ground ($V_1=0, V_2=1$). Calculate the current

vector flowing into this tier through these two ports and then minus vector S . The result is the other column of J :

$$\begin{bmatrix} J_{12} \\ J_{22} \end{bmatrix} = \begin{bmatrix} \frac{\partial I_1}{\partial V_2} \\ \frac{\partial I_2}{\partial V_2} \end{bmatrix}$$

It should be pointed out that the procedure above only needs to factorize G once. The following steps to obtain the Jacobi matrix are all back substitutions. Circuit representation of the port equivalent model is shown in Figure 6. Then we can use the equivalent circuit in Figure 6 to replace the corresponding tier in the global network. The number of nodes in the final network is equal to the total number of ports, which is usually quite small in the clustered TSV location based 3D chips.

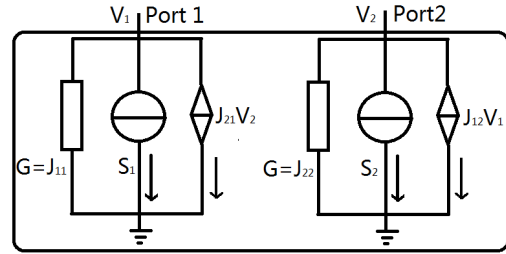


Fig. 6. Circuit representation of the port equivalent model when port number is 2.

When the port number increases, the computing procedure is similar to the above. The only difference is that the number of ports to be scanned to obtain Jacobi matrix increases. As for the circuit representation, with the increase of port number, the voltage-controlled current source (VCCS) number connected to each port will be increasing accordingly.

Benefits of the port equivalent model can be concluded as follows:

- 1) The port equivalent model of each tier can be computed with full parallelism. Besides, when computing the Jacobi matrix J , columns of J are all independent from each other and can also be computed in parallel.
- 2) After replacing all tiers in 3D P/G network with the port equivalent model, the complexity of the global network will be reduced greatly.
- 3) The port equivalent model has the similar advantage as SPRMs mentioned in [12]. To defend the safety of confidential products, most of the chip vendors tend to mask details of implementation. So it is usually unrealistic to obtain detailed P/G information of a commercial chip for designers, which makes it inconvenient to stack chips from different vendors together in the power-integrity aware chip design. To avoid this phenomenon, vendors can provide a port equivalent model of their chip to designers, which can not only defend their products, but also contribute to the 3D chip design.
- 4) The port equivalent model also has the potential to be used in the transient simulation. During the transient simulation, the conductance matrix G keeps the same if the time step is fixed. As the Jacobi matrix reflects the port dependencies and has nothing to do with current sources attached inside the network, it also keeps the same. The port equivalent model only needs to update vector S though one-time back substitution during the simulation. The computation complexity of the back substitution is linear. Although our method can also be extended to the transient simulation, this paper only considers IR drop analysis at present.

TABLE I
VERIFICATION OF THE PROPOSED METHOD ON A 3D P/G BENCHMARK FROM INDUSTRIAL DESIGN

3D-uP (831184 P/G nodes) Number of tiers: 2 TSV clusters: 2×2	Time (s)			Memory (KB)			Max absolute error(V)
	Compute equivalent models	Simulate the global network	Total time	Compute equivalent models	Simulate the global network	Peak memory	
Direct full network simulation	0	1.420	1.420	0	143956	143856	<1.00e-20
Hierarchical approach with full port equivalent models	0.747	0.005	0.752	72050	8500	72050	2.25e-12

IV. SIMPLIFIED PORT EQUIVALENT MODEL

When the number of ports becomes larger, the number of VCCSs in the equivalent model will increase accordingly. If there are a large number of ports, the equivalent model can be very complicated. To solve this problem, we introduce the “locality” property into the hierarchical simulation to simplify the port equivalent model in this section. In the following part, subsection A shows the existence of “locality” effect in 3D chips with the clustered TSV location. Subsection B explains the way to obtain simplified port equivalent models.

A. “Locality” property

In the 2D flip-chip packaging, frequently and uniformly distributed C4 bumps cause a “locality” effect, which means the current is generally drawn from the closest bumps for a particular area [13]. The affected area of one power source in flip-chips is very limited.

In the 3D P/G network with a clustered TSV location, several TSVs are put into a cluster while aligned to C4 bumps in the bottommost tier downwards. TSV clusters play the role of C4 bumps in intermediate tiers. Figure 7 shows the current distribution induced by attaching a unit voltage source to the center port when computing the port equivalent model. We can find the influence of one TSV cluster on the others attenuates very quickly after passing through several clusters. So the “locality” effect also exists in each tier.

B. Simplified port equivalent model

According to the “locality” property of the P/G network, when we attach a unit voltage source to one port, the induced currents on other ports far away from the current one are quite small. That means the Jacobi matrix J in the port equivalent model can be quite sparse when we omit port dependencies between ports far away from each other. As for the circuit representation of the port equivalent model shown in Figure 6, the number of VCCSs will be reduced dramatically when taking the “locality” property into consideration. As will be seen in section VB, we can omit most of the VCCSs while maintaining the accuracy at the same time when the number of ports becomes large. With the “locality” effect, non-zero elements of the Jacobi matrix in simplified models can be only 5% of that in the full port equivalent model.

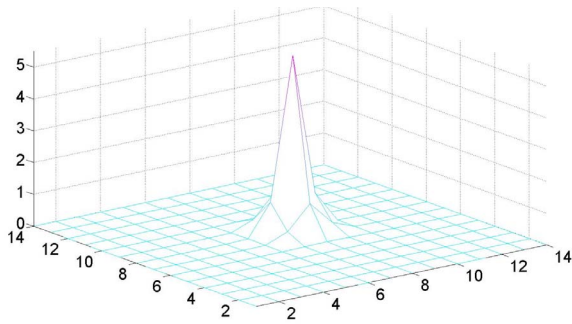


Fig. 7. “Locality” property (Each node in XY plane represents a TSV cluster. Z-coordinate represents the absolute value of current (Ampere) induced by attaching a unit voltage source on the center of the grid.)

V. EXPERIMENTAL RESULTS

In this section, “direct full network simulation” means that the simulation does not use equivalent models and regards all the tiers as a whole. We use it as a baseline in the experiments. “Full port equivalent model” means that the equivalent models used in the hierarchical simulation consider all the port dependencies, while “simplified model” refers to models considering the “locality” property, in which we only care about the port dependencies inside the several surrounding TSV clusters for one port. This paper only focuses on the IR drop analysis at present.

By default, in the following experiments, the wire width is $2.5\mu\text{m}$ in the P/G network and the length between two P/G nodes is set to be $10\mu\text{m}$ [14]. One TSV cluster contains 4×4 TSVs. The network in each tier has a mesh-based topology. The network “ $M\times N\times K$ ” means there are K tiers and each tier contains $M\times N$ power nodes. Besides, power pads on tier1 connect to Vdd (0.8V) through the package. The package is modeled as a lumped resistor here.

The software HS3DPG is implemented using C language. The simulation platform is CentOS4.8 with 2 Intel Xeon X5680 CPUs @3.33GHz (12 cores) and 48GB RAM. Port equivalent models of each tier are computed in parallel. When computing a port equivalent model, in consideration of the hardware platform, columns of the Jacobi matrix are computed using 4 threads here. But it should be noted that columns of the Jacobi matrix can also be computed in full parallel, which could obtain more benefits.

A. Verification and scalability of the proposed approach

This subsection will firstly verify the correctness of our approach and then analyze the scalability of HS3DPG with the increasing of tier number.

TABLE II
SCALABILITY OF THE HIERARCHICAL APPROACH ALONG WITH THE NUMBER OF TIERS

Number of tiers	Direct full network		Full port equivalent model	
	Peak memory (MB)	Total time (s)	Peak memory (MB)	Total time (s)
3	1791.48	82.57	638.30	32.37
6	3533.29	156.15	638.30	32.45
9	5284.70	221.54	638.30	34.09
12	7033.58	303.63	638.30	32.36

Table I shows the simulation results for a 3D P/G network extracted from a real 3D chip of industrial design [20]. This chip has two tiers and 2×2 TSVs. The hierarchical simulation can be about 1.9 times faster than the direct full network simulation. Besides, the peak memory allocated by the direct full network simulation is nearly 2 times that of the hierarchical approach. The accuracy of the hierarchical simulation can also be well maintained (up to 10^{-12}).

Table II illustrates the behavior of our methods when the number of tiers in 3D P/G network increases. In the simulation, each tier contains 1M P/G nodes and 10×10 TSV clusters. The results show that the computational cost of direct full network simulation increases linearly with the tier number, while the proposed hierarchical approach almost costs the same time and peak memory because of parallelism. That is to say, HS3DPG can ensure good scalability with the increase of tier number and gain more benefits when the tier number becomes larger.

TABLE III
 RUNTIME AND MEMORY COMPARISON WHEN THE NUMBER OF TSV CLUSTERS IN EACH TIER INCREASES

1000x1000x3. The number of TSV clusters in each tier changes	Direct full network simulation		Simulation using full port port equivalent models				Simulation using simplified port equivalent models					
	Peak memory (MB)	Total time (s)	Memory (MB)		time (s)		Max absolute error(V)	Memory (MB)		time (s)		Max absolute error(V)
			Compute equivalent models	Simulate the global network	Compute equivalent models	Simulate the global network		Compute equivalent models	Simulate the global network			
	10x10 TSV clusters	1885.26	85.48	611.44	83.54	29.99	0.11	<0.8e-12	611.44	47.42	29.99	0.10
13x13 TSV clusters	1834.93	81.45	635.43	218.40	36.61	0.16	1.01e-12	635.43	82.15	36.60	0.12	2.62e-4
20x20 TSV clusters	1934.30	105.75	655.31	1192.30	51.38	0.38	1.00e-12	655.31	206.81	51.24	0.22	2.24e-4
48x48 TSV clusters	2800.40	352.51	704.47	3381.83	168.88	0.58	1.04e-12	704.47	388.60	167.32	0.30	2.72e-4

For example, when there are 9 tiers, HS3DPG can be 6.5 times faster than the direct full network simulation. The peak memory allocation of the direct full network simulation is nearly 8.3 times larger than HS3DPG.

B. Analysis and performance of simplified port equivalent models

As known in Section IIIB, the number of TSV clusters may have a great impact on the complexity of port equivalent models. This subsection will introduce simplified port equivalent models considering the “locality” property into HS3DPG and evaluate the performance of different approaches when the number of TSV clusters increases.

TABLE IV
 SPARSITY OF THE JACOBI MATRIX

TSV cluster array in each tier	Sparsity of the Jacobi matrix in full port equivalent models	Sparsity of the Jacobi matrix in simplified port equivalent models
10x10	1.00	0.49
13x13	1.00	0.33
20x20	1.00	0.16
25x25	0.9997	0.1076
48x48	0.62	0.032

For a $1000 \times 1000 \times 3$ P/G network, the results when the number of TSV clusters in each tier changes are listed in Table III. During the simulation, simplified port equivalent models only consider the port dependencies inside the surrounding 4×4 TSV clusters for one port. The Jacobi matrix of the simplified model is relatively sparser than the one of full port equivalent models, which means the global network using simplified port equivalent models contains fewer VCCSs. The sparsity of the Jacobi matrix is shown in Table IV. We can find that when the port number becomes large, the simplified model can significantly reduce the nonzero elements in the Jacobi matrix.

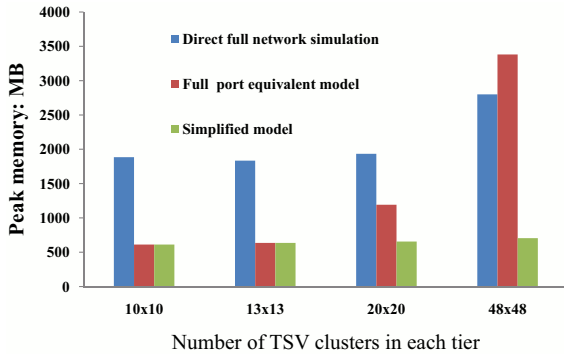


Fig. 8. Peak memory comparison when the number of TSV clusters in each tier changes.

The peak memory and total runtime comparisons in Table III are shown in Figure 8 and Figure 9. We can find that when the number of ports in each tier increases, the peak memory allocation of the hierarchical approach using full port equivalent models also has a significant increase, while the one using simplified models almost keeps the same. For example, when the number of TSV clusters is

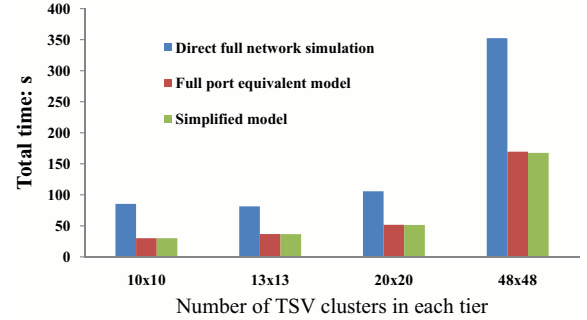


Fig. 9. Total time comparison when the number of TSV clusters in each tier changes.

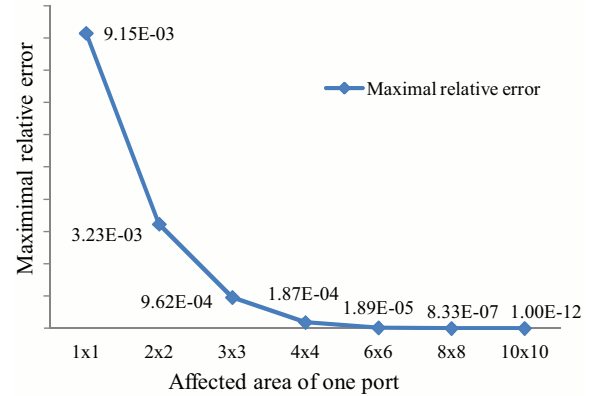


Fig. 10. The maximal relative error of port voltages changes along with the affected area of one port.

48×48 in each tier, the peak memory of the simulation based on full port equivalent models is 4.8 times larger than the one using simplified models. The reason is that the number of VCCSs in full port equivalent models nearly has a quadratic increase along with the number of ports in each tier. These VCCSs will cause large amount of fill-ins when solving the final network. Simplified models have much smaller number of VCCSs because we omit most of the port dependencies. In addition, the hierarchical approach can also achieve more than 2 times acceleration in time consumption under 3 tiers even when the number of TSV clusters becomes quite large (2304 TSV clusters).

In Table III, the computational cost of the network with 10×10 TSVs is larger than that of the network with 13×13 TSVs in the direct full network simulation, which mismatches the intuitive result. That’s because the sparse matrix solver used in this paper uses some optimization techniques to preprocess the established matrix. The performance of the optimization technique varies a little for different matrices. Besides, there is no big difference for the circuit complexity between 10×10 (100) TSVs and 13×13 (169) TSVs. The performance fluctuation of the sparse solver covers the complexity difference between them in the direct full network simulation.

Simplified models considering “locality” effect can reduce the

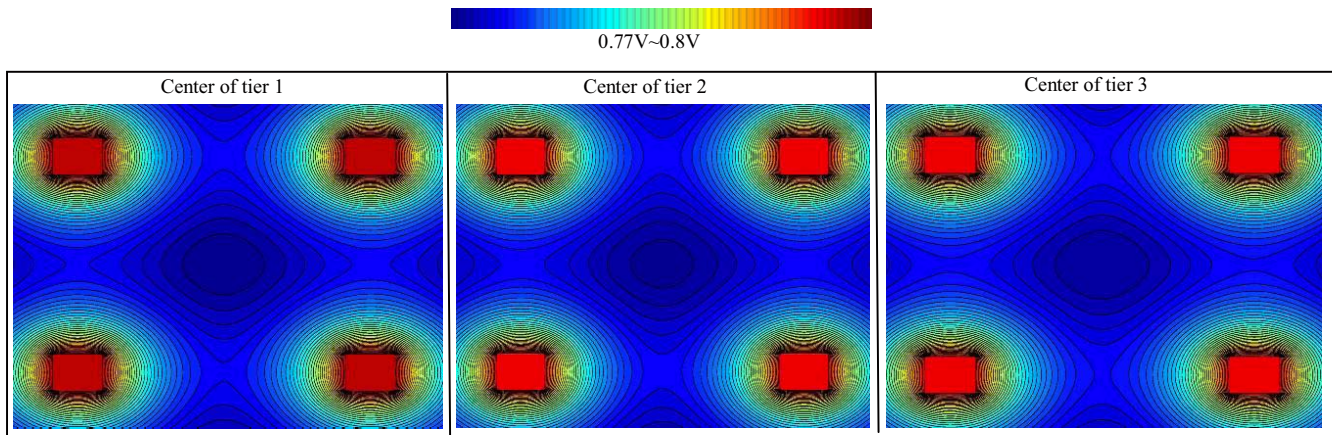


Fig. 11. Voltage distribution maps of different tiers

complexity of simulating the final global network. However it will also reduce the accuracy. Figure 10 shows the maximal relative error of port voltages as the affected area of one TSV cluster changes when computing the simplified model. If we make the affected area of one TSV cluster too small in simplified models, the relative error will be unacceptable. So the user should make a balance when computing simplified port equivalent models.

C. Voltage Distribution of clustered TSV based 3D chips

Figure 11 shows the voltage distribution maps of a 3-tier P/G network with clustered TSVs. The results are generated by HS3DPG. In this experiment, each tier is a 450×450 P/G grid with 10×10 TSV clusters. Parameters of P/G wires are extracted through PTM interconnect models under 45nm technology [14]. The current values attached to each node are randomly generated and the average current density is $64\text{A}/\text{cm}^2$ [21].

In the clustered TSV location based 3D chip, as several TSVs are stacked in one cluster together, the conductance of the vertical connection is quite large. So the IR-drop in the vertical direction along TSVs is small in the clustered architecture. Nodes connected to TSV clusters always have the maximum voltage in each tier. In addition, by comparing the voltage distribution of different tiers, we find the tiers closer to the package have the smaller IR-drop, which is a very intuitive conclusion. However, this phenomenon reminds us to pay particular attention to the power supply on the top tiers in the 3D chip design. When there are too many tiers, besides P/G TSVs, the designers need to explore some other techniques to maintain the voltage constraint of top tiers.

VI. CONCLUSIONS

In this paper, we propose a hierarchical simulation method suitable for 3D P/G network (HS3DPG). The proposed method firstly separates different tiers from the global network and then extracts the port equivalent models in parallel. To further simplify the port equivalent model, we introduce the “locality” property into the 3D P/G network simulation. Experimental results have proven the accuracy and scalability of our method. HS3DPG has significant advantages in terms of memory allocation and time consumption compared with the direct full network simulation. Finally, we use HS3DPG to analyze the voltage distribution map of a clustered TSV based 3D P/G network.

For the future work, we will extend HS3DPG to the transient simulation.

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