The impact of correlation between NBTI and TDDB on the performance of digital circuits

(Invited Paper)

Hong Luo*, Yu Wang*, Jyothi Velamala†, Yu Cao†, Yuan Xie‡ and Huazhong Yang*
*Dept. of E.E., TNList, Tsinghua Univ., Beijing, China
Email: hongluo@tsinghua.edu.cn, yu-wang@tsinghua.edu.cn
†Dept. of ECEE., Arizona State Univ., USA
‡Dept. of CSE, Pennsylvania State Univ., USA

***Abstract*—With integrated circuits scale into the nano-scale era, aging effect becomes one of the most important design challenges. Both the biased temperature instability (BTI) and time-dependent dielectric breakdown (TDDB) can significantly degrade the performance of the circuits. In this paper, we consider the correlation between BTI and TDDB, and apply the correlation model to digital circuit analysis for the first time. The results show that the correlation can lead to 10.42% further more delay degradation.**

***Index Terms*—Aging, BTI, TDDB, Correlation**

I. Introduction

As technology scales down, the BTI and TDDB effects are becoming the most important long-term reliability problems of the gate dielectrics [1]. These two phenomena will degrade the drain current, threshold voltage, and etc. How to overcome these reliability obstacles is a primary concern for researchers and designers. As we known, the negative biased temperature instability (NBTI) effect dominates in pMOS device and positive biased temperature instability (PBTI) dominates in nMOS device. Currently, PBTI effect is minimal compared to NBTI, thus we mainly focus on the correlation between NBTI and TDDB effect in this paper.

The NBTI effect involves interface traps in the gate dielectric, shifts the threshold voltage and finally slows down the devices and circuits [2], [3]. The dissociation of the Si-H bonds due to NBTI can shift the threshold voltage by more than 50mV [4], and then degrades the performance of digital circuits by 15% [5]. The NBTI phenomenon mainly exists in pMOS devices, and is classified as two modes: *static* and *dynamic* NBTI. Static NBTI is involved by the constant voltage stress, and the impact of electric parameters (such as the electric field across the oxide and temperature) on the interface trapping was studied in [2].

Traditionally, the TDDB effect will finally break down the device and make completely conducting in the oxide layer, which is stated as the *hard* breakdown. Currently, another breakdown mode, namely *soft* breakdown becomes a critical concern. In the soft breakdown mode, the oxide layer's insulating properties will degrade aggressively [6], such as 10% degradation in the drain current, and 75mV shift in the threshold voltage [7]. Soft breakdown means the electrical properties of the device will degrade slowly, but the device is still working [8].

This work was supported by the National Natural Science Foundation of China under Contract 60870001 and 61028006. The work of Y. Cao was supported in part by SRC.

Researchers have substantially studied these aging effects, but the correlation between them is not studied thoroughly. Recently, the correlation between NBTI and TDDB is reported [9], which showed that NBTI induced defects are somewhat identical to the defects that dominate the breakdown process. However, the impact of the correlation effect on the circuit performance is not published yet. This paper shows the contribution in the following aspects:

- This paper models the correlation effect between NBTI and TDDB. The model shows that the impact of the correlation effect increases as the NBTI and TDDB effect become more severe.
- The model can be used for circuit analysis. The analysis demonstrates that the correlation effect will further slow down the circuit, and the difference can be 9.01% of delay degradation in average.

The rest of this paper is organized as follows. Section II reviews related works including both NBTI and TDDB models. Section III proposes our model of the correlation effect between NBTI and TDDB. In Section IV, the correlation model is applied to analyze the performance degradation of the digital circuits, and the impact of the correlation effect on the circuit delay is demonstrated. Finally, Section V concludes the paper.

II. Related work

The physics of NBTI effect is related to the interface trap generation in oxide layer, and can be described by the reaction-diffusion (R-D) model [10]. The shift in the threshold voltage due to the NBTI effect is proportional to the interface trap generation N_{it} [11]. Paul et al. analyze the impact of NBTI on the worst case performance degradation of digital circuits [11]. The predictive NBTI model for various process and design parameters was proposed in [12], [13]. Analytical models for dynamic NBTI were proposed in [14], [15]. The temperature-

978-1-61284-857-0/11/$26.00

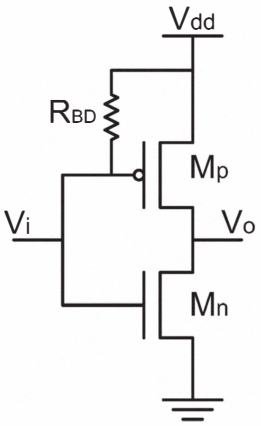

Fig. 1. Breakdown resistance in pMOS device in the inverter

aware NBTI model and gate-level model considering the stacking effect are proposed in [15] and [16] respectively.

The hard breakdown mode of TDDB was studied to describe the failure characteristic in a set of devices [6], [7], [17]. Recently, researchers devoted themselves to soft breakdown mode because of its significant implication on oxide reliability. The principles of area, thickness, voltage scaling for soft breakdown were investigated [18]. A model for describing multiple soft breakdown events in ultra-thin gate dielectrics was proposed in [19]. The impact of TDDB on the stability of digital circuits was investigated in [20], and SRAM stability due to TDDB was addressed in [8], [21]. An accurate analytical model to predict the delay of logic gates subject to TDDB was proposed in [22], which can be seamlessly integrated into a static timing analysis tool. In [23], the output degradation of TDDB effect is considered, and shows a possible boost up of the circuit performance.

A. NBTI model

The threshold voltage degradation ΔV_{th} due to NBTI can be calculated as [13]

$$\Delta V_{\text{th}} = K_{\text{V}} \cdot t^{\frac{1}{6}} \tag{1}$$

where

$$K_{\text{V}} = \left(\frac{qT_{\text{ox}}}{\varepsilon_{\text{ox}}}\right) \sqrt[3]{K^2 C_{\text{ox}}(V_{\text{gs}} - V_{\text{th}})\sqrt{C}\exp\left(\frac{2E_{\text{ox}}}{E_0}\right)} \tag{2}$$

and these parameters are the same as defined in [13].

B. TDDB model

The "R-model" is commonly used for TDDB analysis in circuits. In order to model the impact of soft breakdown on digital circuits, the increasing gate leakage I_{gate} is modeled as a breakdown resistance between the gate and drain/source [22], as shown the resistor R_{BD} in Fig. 1. Based on the experiments and published data, the resistance ranges from hundreds of MΩ (fresh oxide) to a few kΩ (hard breakdown) [20], [22]. In this paper, because we only consider the correlation between NBTI (in pMOS) and TDDB, the breakdown resistance is connected in pMOS device of the inverter as shown in Fig. 1

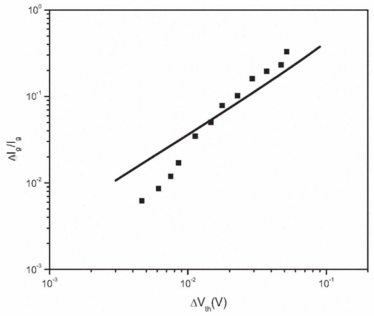

Fig. 2. Shift in gate current as a function of threshold voltage shift

III. Correlation analysis between NBTI and TDDB

As we know, the soft breakdown effect relates to the increase of the gate tunneling leakage current I_g. And this current depends on the gate-to-source voltage V_{gs}, which is given by

$$I_g \sim A \cdot \exp(B \cdot V_{gs}) \tag{3}$$

where V_{gs} can be increased by the trapped charge, which can be described by the following

$$V_{gs,trap} = V_{gs} + K \cdot \frac{Q_t}{C_{ox}} \tag{4}$$

The NBTI effect is also related with trapped charge, and the shift of threshold voltage can be calculated as

$$\Delta V_{th} = \frac{Q_t}{C_{ox}} \tag{5}$$

Therefore, there is correlation between the gate current (TDDB) and threshold voltage shift (NBTI).

A. Correlation model

From the data extracted from physical experiment shown in Fig. 2, we find that

$$\log_{10}\left(\frac{\Delta I_g}{I_g}\right) = \gamma \cdot \log_{10}(\Delta V_{th}) + \beta \tag{6}$$

Then, we can get

$$\frac{\Delta I_g}{I_g} = 10^{\beta} \cdot (\Delta V_{th})^{\gamma} = \kappa \cdot (\Delta V_{th})^{\gamma} \tag{7}$$

With the 45nm experimental data as shown in Fig. 2, we have $\kappa \approx 4.8$ and $\gamma \approx 1$. We can calculate that the increase of gate current can reach up to 42.8%, when threshold voltage shifts by 100mV.

For TDDB modeling, we use the "R-model" shown in Fig. 1, and model the correlation effect for the breakdown resistance,

$$R_{BD,corr} = R_{BD}/(1 + \kappa \cdot (\Delta V_{th})^{\gamma}) \tag{8}$$

where $R_{BD,corr}/R_{BD}$ are breakdown resistance with/without correlation, respectively.

B. Delay model with correlation effect

In the last section, we have created the model of the correlation effect between NBTI and TDDB. This section proposes the delay model of these two aging effect.

The NBTI effect shifts the threshold voltage of PMOS device, and leads to a longer charging time to the output node. While, the TDDB effect will raise the input voltage of the logic 0 [23], and thus reduce the voltage swing too.

The degradation of the voltage swing ΔV_{BD} can be also expressed as [23]

$$\Delta V_{BD} = \frac{R_{eq}}{R_{BD}} \cdot V_{dd} \tag{9}$$

where R_{eq} can be taken as equivalent resistance of the pull-down network of fan-in gate.

Thus, if we do not consider the correlation between NBTI and TDDB, the charing current (saturation current of PMOS) can be expressed as

$$I_{dsat} = \upsilon_{sat} C_{ox} W (V_{dd} - \Delta V_{BD} - V_{th} - \Delta V_{th} - \frac{V_{dsat}}{2}) \tag{10}$$

where ΔV_{th} and ΔV_{BD} are degradation due to NBTI and TDDB, respectively.

The delay degradation can be given by

$$\Delta t_p \approx t_p \cdot \frac{\Delta V_{BD} + \Delta V_{th}}{V_{dd} - V_{th} - V_{dsat}/2} \approx t_p \cdot \frac{\Delta V_{BD} + \Delta V_{th}}{V_{dd}} \tag{11}$$

where ΔV_{BD} is the voltage swing degradation considering no correlation.

From Eq. (8) and (9), the degradation of voltage swing considering the correlation between NBTI and TDDB can be expressed by

$$\begin{aligned} \Delta V_{BD,corr} &= \frac{R_{eq} V_{dd}}{R_{BD}/(1 + \kappa \cdot (\Delta V_{th})^{\gamma})} \\ &= (1 + \kappa \cdot (\Delta V_{th})^{\gamma}) \Delta V_{BD} \end{aligned} \tag{12}$$

Therefore, if the correlation effect is considered, the degradation can be expressed as

$$\Delta t_p = t_p \cdot \frac{\Delta V_{th} + \Delta V_{BD} + \kappa \cdot (\Delta V_{th})^{\gamma} \cdot \Delta V_{BD}}{V_{dd}} \tag{13}$$

From the above equation, we can conclude that the correlation effect will increase the delay, because ΔV_{BD} and ΔV_{th} are both positive values.

The simulation is performed to validate the correlation model. Fig. 3 shows that the correlation between NBTI and TDDB can increase the delay, and the correlation effect becomes larger as V_{th} increases. This shows the consistency with our model described by Eq. (13).

IV. Delay Analysis for Digital Circuits

In this section, we will consider the correlation between NBTI and TDDB in circuit performance analysis.

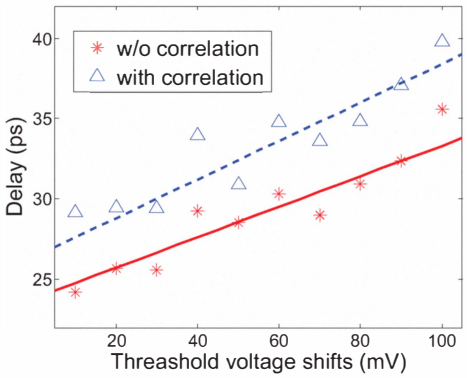

Fig. 3. Comparison of the delay with and w/o considering the correlation

In circuit performance analysis, we will use the gate-level delay model. The delay of a gate υ can be expressed as [24]

$$\begin{aligned} d(\upsilon) &= \frac{K}{(V_{gs} - V_{th})^{\alpha}} \\ K &= \frac{C_L V_{dd}}{\mu C_{ox} W_{eff}/L_{eff}} \end{aligned} \tag{14}$$

where α is the velocity saturation index, which ranges from 1 to 2, and depends on the type of logic gate.

If the aging effects (including both NBTI and TDDB) are considered, the delay degradation should be

$$\Delta d(\upsilon) = d(\upsilon) \cdot \frac{\alpha \Delta V_{age}}{V_{gs} - V_{th}} \tag{15}$$

where ΔV_{age} is the degradation of V_{gs} due to the aging effect. If no correlation is considered, the degradation $\Delta V_{age} = \Delta V_{BD} + \Delta V_{th}$. If we consider the correlation between NBTI and TDDB, the degradation of V_{gs} should be expressed as

$$\Delta V_{age} = \Delta V_{BD} + \Delta V_{th} + \kappa \Delta V_{BD} (\Delta V_{th})^{\gamma} \tag{16}$$

where $\gamma \approx 1$, thus we can get that

$$\Delta V_{age} = \Delta V_{BD} + \Delta V_{th} + \kappa \cdot \Delta V_{BD} \cdot \Delta V_{th} \tag{17}$$

Thus, we can estimate the delay degradation considering the correlation between NBTI and TDDB effect.

In this section, the ISCAS85 circuits are used as the benchmark. In this paper, the standard cell library is constructed using the PTM 45nm bulk CMOS model [25]. $V_{dd} = 0.8$V, $|V_{th}| = 200$mV are set for all the transistors in the circuits.

Fig. 4 shows the impact of the correlation between NBTI and TDDB on the performance of C1355 benchmark circuit. The threshold voltage shifts in the logic gates are simulated by the model proposed in [15], and the input voltage degradation of the gate (ΔV_{BD}) are set randomly ranging from 5mV to 150mV. In Fig. 4, the delay degradation without considering the correlation is treated as the reference (considered as 0%), and the results are the normalized variation of the delay degradation considering the correlation. In average, the correlation between NBTI and TDDB leads to 9.36% more delay degradation.

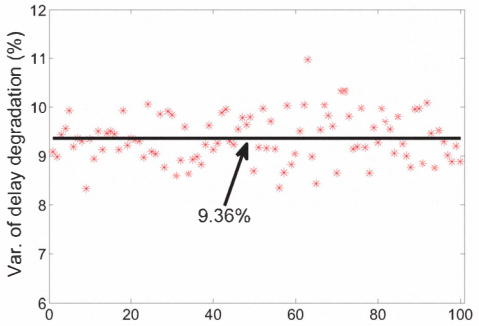

Fig. 4. Variation of the delay degradation in C1355 considering the correlation (the delay degradation without correlation is taken as 0%)

TABLE I
DELAY DEGRADATION OF ISCAS85 BENCHMARK CIRCUITS CONSIDERING THE CORRELATION BETWEEN NBTI AND TDDB

ISCAS85 Circuits	Nominal delay (ns)	No corr. Δd (%)	Corr. Δd (%)	Var. of Δd (%)
c432	4.99	4.97	5.43	9.26
c499	1.98	4.75	5.16	8.63
c880	3.39	6.30	6.86	8.89
c1355	3.82	8.33	9.11	9.36
c1908	4.58	6.60	7.21	9.24
c2670	4.71	8.34	9.13	9.47
c3540	6.04	9.12	10.07	10.42
c5315	6.26	8.37	9.16	9.44
c6288	21.1	7.52	8.12	7.98
c7552	6.49	9.95	10.69	7.44
Average	N/A	N/A	N/A	9.01

In Table I, the same approach is applied to all the ISCAS85 benchmark circuits. The results show that the correlation between NBTI and TDDB can degrade further more 9.01% of the delay degradation in average, and the maximum difference can be 10.42%.

V. CONCLUSION

This paper considers the correlation effect of NBTI and TDDB effect, which is the severest aging effect currently. The correlation model used in digital circuit analysis is proposed. This model is applied to circuit performance estimation, and the results show that the correlation can lead to on average 9.01% more delay degradation. The PBTI effect may become predominant and comparable to NBTI, and the similar approach can be applied to analyzing the correlation between PBTI and TDDB.

REFERENCES

[1] A. Ghetti, "Gate oxide reliability: Physical and computational models," in *Predictive simulation of semiconductor processing: status and challenges*, ser. Springer Series in Materials Science, J. Dabrowski and E. R. Weber, Eds. Springer, 2004, pp. 201–258.

[2] M. A. Alam and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," *Microelectronics Reliability*, vol. 45, no. 1, pp. 71 – 81, 2005.

[3] S. Mahapatra, D. Saha, D. Varghese, and P. Kumar, "On the generation and recovery of interface traps in MOSFETs subjected to NBTI, FN, and HCI stress," *IEEE Transactions on Electron Devices*, vol. 53, no. 7, pp. 1583 –1592, jul. 2006.

[4] L. Peters, "NBTI: A Growing Threat to Device Reliability," *Semiconductor International*, vol. 27, no. 3, Mar. 2004.

[5] K. Bernstein, D. J. Frank, A. E. Gattiker, W. Haensch, B. L. Ji, S. R. Nassif, E. J. Nowak, D. J. Pearson, and N. J. Rohrer, "High-performance CMOS variability in the 65-nm regime and beyond," *IBM J. Res. & Dev.*, vol. 50, no. 4/5, pp. 433–449, 2006.

[6] M. Alam, B. Weir, J. Bude, P. Silverman, and A. Ghetti, "A computational model for oxide breakdown: theory and experiments," *Microelectronic Engineering*, vol. 59, no. 1-4, pp. 137 – 147, 2001.

[7] A. Haggag, M. Moosa, N. Liu, D. Burnett, G. Abeln, M. Kuffler, K. Forbes, P. Schani, M. Shroff, M. Hall, C. Paquette, G. Anderson, D. Pan, K. Cox, J. Higman, M. Mendicino, and S. Venkatesan, "Realistic projections of product fails from NBTI and TDDB," in *Proc. 44th Annual. IEEE Int Reliability Physics Symp*, 2006, pp. 541–544.

[8] B. Kaczer, R. Degraeve, P. Roussel, and G. Groeseneken, "Gate oxide breakdown in FET devices and circuits: From nanoscale physics to system-level reliability," *Microelectronics Reliability*, vol. 47, no. 4-5, pp. 559 – 566, 2007, 14th Workshop on Dielectrics in Microelectronics (WoDiM 2006).

[9] N. Rahim and D. Misra, "Correlation of negative bias temperature instability and breakdown in HfO2/TiN gate stacks," *ECS Transactions*, vol. 28, no. 2, pp. 323–330, 2010.

[10] S. Ogawa and N. Shiono, "Generalized diffusion-reaction model for the low-field charge-buildup instability at the Si-SiO_2 interface," *Physical Review B*, vol. 51, no. 7, pp. 4218–4230, 1995.

[11] B. Paul, K. Kang, H. Kufluoglu, M. Alam, and K. Roy, "Impact of NBTI on the temporal performance degradation of digital circuits," *IEEE Electron Device Letters*, vol. 26, no. 8, pp. 560–562, 2005.

[12] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and Minimization of PMOS NBTI Effect for Robust Nanometer Design," in *Proc. of DAC*, 2006, pp. 1047–1052.

[13] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, and S. Vrudhula, "Predictive Modeling of the NBTI Effect for Reliable Design," in *Proc. of CICC*, 2006, pp. 189–192.

[14] S. Kumar, C. Kim, and S. Sapatnekar, "An Analytical Model for Negative Bias Temperature Instability," in *Proc. of ICCAD*, 2006, pp. 493–496.

[15] H. Luo, Y. Wang, R. Luo, H. Yang, and Y. Xie, "Temperature-aware NBTI modeling techniques in digital circuits," *IEICE Transactions on Electronics*, vol. E92-C, no. 6, pp. 875–886, 2009.

[16] H. Luo, Y. Wang, K. He, R. Luo, H. Yang, and Y. Xie, "A novel gate-level NBTI delay degradation model with stacking effect," in *PATMOS*, ser. LNCS. Springer, 2007, vol. 4644, pp. 160–170.

[17] K. Chopra, C. Zhuo, D. Blaauw, and D. Sylvester, "A statistical approach for full-chip gate-oxide reliability analysis," in *Proc. of ICCAD*, nov. 2008, pp. 698 –705.

[18] M. Alam, B. Weir, and P. Silverman, "A study of soft and hard breakdown - Part II: Principles of area, thickness, and voltage scaling," *IEEE Transactions on Electron Devices*, vol. 49, no. 2, pp. 239 –246, feb. 2002.

[19] M. Alam and R. Smith, "A phenomenological theory of correlated multiple soft-breakdown events in ultra-thin gate dielectrics," in *Proc. of IRPS*, 2003, pp. 406 – 411.

[20] B. Kaczer, R. Degraeve, M. Rasras, K. Van de Mieroop, P. Roussel, and G. Groeseneken, "Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability," *IEEE Transactions on Electron Devices*, vol. 49, no. 3, pp. 500 –506, mar. 2002.

[21] R. Rodriguez, J. Stathis, B. Linder, S. Kowalczyk, C. Chuang, R. Joshi, G. Northrop, K. Bernstein, A. Bhavnagarwala, and S. Lombardo, "The impact of gate-oxide breakdown on SRAM stability," *IEEE Electron Device Letters*, vol. 23, no. 9, pp. 559 – 561, sep. 2002.

[22] M. Choudhury, V. Chandra, K. Mohanram, and R. Aitken, "Analytical model for TDDB-based performance degradation in combinational logic," in *Proc. of DATE*, 2010, pp. 423–428.

[23] H. Luo, X. Chen, J. Velamala, Y. Wang, Y. Cao, V. Chandra, Y. Ma, and H. Yang, "Circuit-level delay modeling considering both TDDB and NBTI," in *International Symposium on Quality Electronic Design (ISQED)*, 2011, pp. 14 – 21.

[24] B. Paul, K. Kang, H. Kufluoglu, M. Alam, and K. Roy, "Temporal Performance Degradation under NBTI: Estimation and Design for Improved Reliability of Nanoscale Circuits," in *Proc. of DATE*, 2006, pp. 780–785.

[25] Nanoscale Integration and Modeling (NIMO) Group, ASU, "Predictive Technology Model (PTM)." [Online]. Available: http://www.eas.asu.edu/~ptm/