

Circuit-level delay modeling considering both TDDB and NBTI

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Abstract—With aggressive scaling down of the technology node, the time-dependent dielectric breakdown (TDDB) and negative biased temperature instability (NBTI) are becoming key challenges for circuit designers. Both TDDB and NBTI significantly degrade the electrical characteristic of the CMOS devices. A delay model considering TDDB and NBTI is proposed in this paper. The output degradation of the breakdown gate is considered in circuit-level delay analysis. Traditionally, it is considered the TDDB degradation always degrades the circuit delay. However, this paper shows the TDDB effect may boost up the circuit speed. The spatial correlation of TDDB effect is also demonstrated in this paper and shows the difference of 40% in circuit delay depending on the location of the breakdown gate in the signal path.

I. INTRODUCTION

With technology scaling down, the aging effect and long-term reliability of the gate dielectrics are becoming key challenges for circuit designers [1]. During the working life of devices, many physical phenomena will degrade the electrical parameters such as drain current and threshold voltage. In this paper, TDDB and NBTI are addressed because of their severity in nano-scale devices.

Firstly, the TDDB effect will degrade the oxide layer's insulating properties aggressively, and finally make completely conducting between gate and substrate [2]. The TDDB effect can degrade the drain current of the device by 10%, and shift the threshold voltage by 75mV [3]. Two TDDB modes have been investigated: *hard* and *soft* breakdown. Hard breakdown exhibits an abrupt increase of gate leakage current, and leads to a catastrophic failure for the device and the entire circuit [4]. Soft breakdown means the electrical properties of the device will degrade slowly, but the device is still working [5]. Besides, TDDB occurs on both nMOS and pMOS, but TDDB in pMOS is at least an order lower than in nMOS because of their different energy band height. Therefore, this paper is focused on the TDDB effect in nMOS devices.

Secondly, another reliability issue is the slowdown of devices due to progressive interface trapping, which is referred

This work was supported by National Key Technology Program of China under Contract 2008ZX01035-001, by the National Natural Science Foundation of China under Contract 60870001. The work of Y. Cao was supported in part by SRC.

to as NBTI [6]. The negative bias of the device causes the dissociation of the Si-H bonds, and yields interface traps, thus shifts the threshold voltage of the transistor [7]. The NBTI effect can shift the threshold voltage by more than 50mV [8], and the performance degradation of the digital circuits can reach up to 15% [9]. The NBTI phenomenon exists in pMOS devices, and is classified as two degradation modes: *static* and *dynamic* NBTI. Static NBTI is involved by the constant voltage stress [6]. Dynamic NBTI corresponds to the AC voltage stress condition, which leads to a less severe parameter's shift because of the recovery phenomenon [7].

Currently, TDDB physics has been widely researched already [10]–[13], while the impact of TDDB on the digital circuits has been less studied. The SRAM stability involved by TDDB was investigated in [5], [14], and an analytical TDDB model to evaluate the circuit delay was introduced in [15]. Besides, considering both TDDB and NBTI effect was mainly applied to SRAM cell [16]. Our contribution in this paper distinguishes itself in the following aspects:

- This paper proposes a circuit-level TDDB delay model. The analytical model in [15] only considered the input degradation due to TDDB. Our model has considered the factor of the output degradation, which leads to 10% difference in total circuit delay. Traditionally, it is considered the circuit delay should always degrade by TDDB, but our circuit delay model shows the TDDB effect may sometimes boost up the circuit speed. Our analysis for the ring oscillator demonstrates the oscillator boosts up 12% in performance if all inverters have breakdown.
- The spatial correlation of TDDB is also demonstrated in this paper. The location where the breakdown occurred in the signal path may significantly affect the overall delay variation of the circuit, while the difference can be 40% in the circuit delay.
- Both TDDB and NBTI effects are considered in our circuit-level delay model, and their impact on the temporal performance variation in digital circuits is studied.

The rest of this paper is organized as follows. Section II reviews related works including both TDDB and NBTI models. Section III proposes our delay model considering both

TDDB and NBTI. In Section IV, the impact of considering the output degradation, and the spatial correlation of TDDB effect is demonstrated, then the impact of both TDDB and NBTI on circuit performance is studied. Finally, Section V concludes the paper.

II. RELATED WORKS

In general, trap generation is the key factor for the oxide breakdown [10], [11]. The anode hole injection (AHI) model [10] and thermo-chemical model [11] were proposed to describe the trap generation. In AHI model, the field dependence can be described by 1/E-model [10], [12], while in the thermo-chemical model, E-model was used [11], [17].

Traditionally, the hard breakdown of TDDB was studied to describe the failure characteristic in a set of devices. The computational model for the oxide breakdown was proposed in [2], where the hole-induced degradation model was used to describe the time to breakdown under different voltages. In [18], a statistical approach for analyzing full-chip TDDB lifetime characteristic was proposed. Realistic projections of the device fail contributed by both NBTI and TDDB were demonstrated on high performance microprocessors in [3].

Recently, soft breakdown has been extensively investigated because of its significant implication on oxide reliability. The theory of percolation conductance was applied to explain the hard and soft breakdown phenomena [13], and the principles of area, thickness, voltage scaling for both hard and soft breakdown were investigated [19]. A model for describing multiple soft breakdown events in ultra-thin gate dielectrics was proposed in [20]. The impact of TDDB on the stability of digital circuits was investigated in [21], and SRAM stability due to TDDB was addressed in [5], [14]. An accurate analytical model to predict the delay of logic gates subject to TDDB was proposed in [15], which can be seamlessly integrated into a static timing analysis tool. The coupled effects of NBTI and TDDB in an SRAM cell were investigated in [16].

It is commonly believed that the reaction-diffusion (R-D) model [22] describes the physics of interface trap generation in NBTI. The NBTI effect leads to the shift in the threshold voltage, which is the key factor in evaluating performance degradation due to NBTI and is proportional to the interface trap generation [23]. Paul et al. analyze the impact of NBTI on the worst case performance degradation of digital circuits [23]. Analytical models for dynamic NBTI were proposed in [24], [25]. The predictive NBTI model for various process and design parameters was proposed in [26], [27]. The temperature-aware NBTI model and gate-level model considering the stacking effect are proposed in [25] and [28] respectively.

A. TDDB model

Oxide soft breakdown degrading the electrical properties of the device is a major concern in current technology nodes [13], [19]. In order to model the impact of soft breakdown on digital circuits, the increasing gate leakage I_{gate} is modeled as a breakdown resistance between the gate and the source [15], as shown the resistor R_{BD} in Fig. 1. Based on the experiments

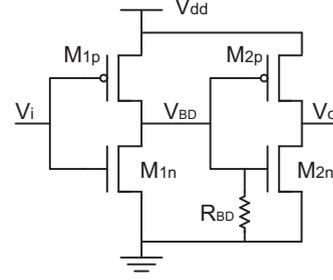


Fig. 1. Breakdown equivalent circuit model

and published data, the resistance ranges from hundreds of $M\Omega$ (fresh oxide) to a few $k\Omega$ (hard breakdown) [15], [21], [29]. This “R-model” is also used in our later analysis.

B. NBTI model

The threshold voltage degradation ΔV_{th} due to NBTI can be calculated as [27]

$$\Delta V_{\text{th}} = K_V \cdot t^{\frac{1}{6}} \quad (1)$$

where

$$K_V = \left(\frac{qT_{\text{ox}}}{\varepsilon_{\text{ox}}} \right)^3 \sqrt[3]{K^2 C_{\text{ox}} (V_{\text{gs}} - V_{\text{th}}) \sqrt{C} \exp\left(\frac{2E_{\text{ox}}}{E_0}\right)} \quad (2)$$

and these parameters are as defined in [27].

III. DELAY MODEL CONSIDERING BOTH TDDB AND NBTI

We have reviewed both TDDB and NBTI models used in this paper. In this section, these models are used to construct our circuit-level delay model. In combinational digital circuits, the TDDB effect will degrade the node voltage swing. Thus, we will analyze the voltage degradation in Section III-A, and the delay variation due to TDDB will be estimated in Section III-B.

A. Model of voltage swing degradation

As shown in Fig. 1, the existence of R_{BD} decreases the voltage swing of V_{BD} . Because the breakdown effect only exists for high voltage stress, our analysis is applied on the scheme that V_{BD} is logic 1, thus V_i is logic 0, and $V_{\text{BD}} < V_{\text{dd}}$ because of the current along R_{BD} .

In the steady state, the transistors M_{1n} , M_{2p} and M_{2n} are almost cut-off, and the current I_{BD} flows from V_{dd} to ground along M_{1p} and R_{BD} .

In the transistor M_{1p} , the current I_{BD} is expressed as

$$I_{\text{BD}} = -\mu_0 C_{\text{ox}} \frac{W}{L} \left[(V_{\text{dd}} - V_{\text{thp}}) V_{\text{ds,1p}} + \frac{V_{\text{ds,1p}}^2}{2} \right] \quad (3)$$

where μ_0 is carrier mobility, C_{ox} is the gate oxide capacitance, W and L represent the channel width and length, V_{thp} is the threshold voltage for pMOS transistor, and $V_{\text{ds,1p}}$ is the drain-to-source voltage of M_{1p} .

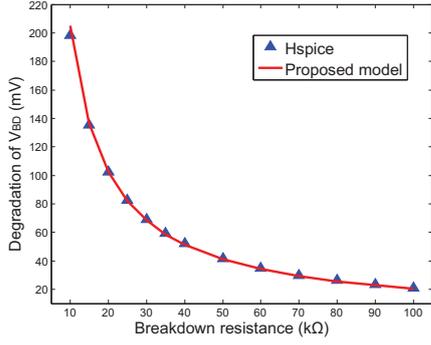


Fig. 2. Degradation of voltage swing due to breakdown resistance

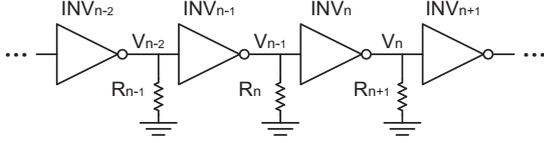


Fig. 3. Inverter chain schematic

Meanwhile, the current I_{BD} can be also expressed as

$$I_{BD} = \frac{V_{dd} + V_{ds,1p}}{R_{BD}} \quad (4)$$

From Eq. (3) and (4), we can solve $V_{ds,1p}$ from

$$\frac{\kappa R_{BD}}{2} \cdot V_{ds,1p}^2 + [1 + \kappa R_{BD}(V_{dd} - V_{thp})] \cdot V_{ds,1p} + V_{dd} = 0 \quad (5)$$

where $\kappa = \mu_0 C_{ox} W/L$.

Because R_{BD} is fairly large and V_{BD} is logic 1, $|V_{ds,1p}| \ll V_{dd}$, $\kappa R_{BD} V_{ds,1p}^2/2$ can be neglected, and $\kappa R_{BD} \gg 1$, we can directly get the drain-to-source voltage of M_{1p}

$$V_{ds,1p} \approx -\frac{V_{dd}}{1 + \kappa R_{BD}(V_{dd} - V_{thp})} \approx -\frac{V_{dd}}{\kappa R_{BD}(V_{dd} - V_{thp})} \quad (6)$$

This model can be validated by Hspice simulation as shown in Fig. 2. The degradation of V_{BD} in this figure is $|V_{ds,1p}|$. Thus, we can conclude the degradation of voltage swing

$$\Delta V_{BD} = \frac{R_{eq}}{R_{BD}} \cdot V_{dd} \quad (7)$$

where $R_{eq} = 1/[\kappa(V_{dd} - V_{thp})]$, which can be considered as the effective resistance of the M_{1p} . We can also extend this model to the general gate logic circuit, where R_{eq} can be replaced by the effective resistance of the pull-up network of the logic gate.

B. Delay model of TDDB

As described above, the breakdown effect degrades the node voltage in circuits, and thus leads to the delay variation. In this section, we will propose an analytical model for estimating the delay variation of logic gate. In order to simplify our derivation, we perform our analysis on the inverter chain.

As shown in Fig. 3, the delay variation of the node voltage V_n is investigated, and similar mechanism was described

in [30]. The breakdown resistance in the inverter INV_n is denoted as R_n , which degrades the voltage swing of V_{n-1} .

For the rising transition of INV_n , the propagation delay is given as

$$t_{pr,n} = \int_0^{V_{dd}/2} \frac{C_{L,n}(V)}{I_{p,n}(V)} dV \approx \frac{C_L V_{dd}}{2I_{dsatp,n}} \quad (8)$$

where $C_{L,n}$ is the effective capacitance of the node V_n , and $I_{p,n}$ is the charging current mainly provided by the pMOS transistor of INV_n . In first-order analysis, we consider that $I_{p,n}$ remains constant as $I_{dsatp,n}$, which is the saturation current of pMOS transistor in INV_n , and the effective capacitance can be considered as the constant C_L for all nodes.

Similarly, the delay for the falling transition is given as

$$t_{pf,n} = -\int_{V_{dd}}^{V_{dd}/2} \frac{C_{L,n}(V)}{I_{n,n}(V)} dV \approx \frac{C_L V_{dd}}{2I_{dsatn,n}} \quad (9)$$

where $I_{n,n}$ is the discharging current mainly provided by the nMOS transistor of INV_n , and $I_{dsatn,n}$ is the saturation current of nMOS transistor of INV_n .

1) *Delay variation with ΔV_{n-1}* : Intuitively, the degradation of V_{n-1} does not affect $t_{pr,n}$, since $I_{dsatp,n}$ remains almost the same. On the other hand, the degradation of $I_{dsatn,n}$ leads to the increase of $t_{pf,n}$.

The saturation current $I_{dsatn,n}$ can be described by

$$I_{dsatn,n} = v_{sat} C_{ox} W (V_{dd} - \Delta V_{n-1} - V_{thn} - \frac{V_{dsatn}}{2}) \quad (10)$$

where v_{sat} is the saturation velocity of nMOS transistor, V_{thn} is the threshold voltage of nMOS, V_{dsatn} is the saturation drain voltage of nMOS, and ΔV_{n-1} is the degradation of the input voltage of INV_n .

Since the degradation $\Delta V_{n-1} \ll V_{dd}$, we can derive the new propagation delay

$$t_{pf,n}^* \approx \frac{C_L V_{dd}}{2v_{satn} C_{oxn} W \cdot V_{gt}} \left(1 + \frac{\Delta V_{n-1}}{V_{gt}}\right) \quad (11)$$

where $V_{gt} = V_{dd} - V_{thn} - V_{dsatn}/2$.

Therefore, the increase of the propagation delay for the falling transition is given by

$$\Delta t_{pf,n} = \frac{\Delta V_{n-1} \cdot t_{pf,n}}{V_{dd} - V_{thn} - V_{dsatn}/2} \approx \frac{\Delta V_{n-1} \cdot t_{pf,n}}{V_{dd}} \quad (12)$$

where ΔV_{n-1} can be estimated by the value of R_n according to Eq. (6).

The above Eq. (12) can be verified by Hspice simulation. In Fig. 4(a), the Hspice simulation results show the delay variation is approximately linear with the degradation of V_{n-1} , when ΔV_{n-1} is less than 140mV.

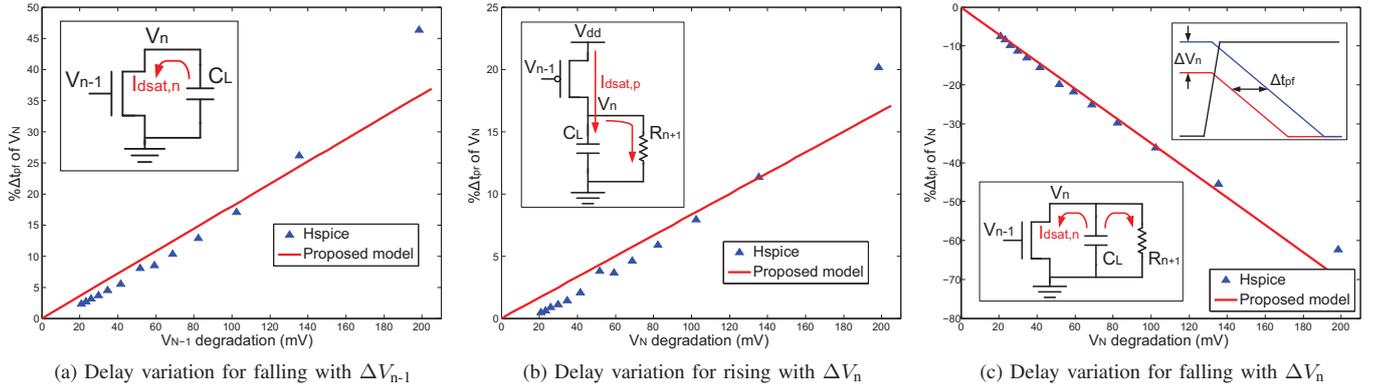


Fig. 4. Delay model verified by Hspice simulation

2) *Delay variation with ΔV_n* : The existence of R_{n+1} can also affect the propagation delay of INV_n . In the following statement, the impact of the output degradation on the delay variation is investigated.

Firstly, we investigate the delay for the rising transition. When the current $I_{dsatp,n}$ charges the node capacitance C_L , a portion of the current is bypassed by R_{n+1} , thus the delay for the rising transition can be expressed by

$$t_{pr,n}^* = \int_0^{V_{dd}/2} \frac{C_L}{I_{dsatp,n} - V/R_{n+1}} dV \quad (13)$$

At the regime of $V/R_{n+1} \ll I_{dsatp,n}$, we can derive that

$$t_{pr,n}^* = \frac{C_L}{I_{dsatp,n}} \int_0^{V_{dd}/2} \left(1 + \frac{V}{I_{dsatp,n} R_{n+1}}\right) dV \quad (14)$$

Thus the increase of the delay can be calculated by

$$\Delta t_{pr,n} = \frac{V_{dd} \cdot t_{pr,n}}{4I_{dsatp,n} R_{n+1}} \quad (15)$$

According to the analysis in Section III-A, the voltage degradation of V_n can be also estimated. From Eq. (7), we get that

$$\Delta V_n = \frac{R_{eqp} V_{dd}}{R_{eqp} + R_{n+1}} \approx \frac{R_{eqp} V_{dd}}{R_{n+1}} \quad (16)$$

where R_{eqp} can be expressed by $V_{dsatp}/I_{dsatp,n}$ in the first-order approximation. From Eq. (15), we can derive that

$$\Delta t_{pr,n} = \frac{\Delta V_n \cdot t_{pr,n}}{4V_{dsatp}} \quad (17)$$

At the regime of $\Delta V_n < 140\text{mV}$, this model can be verified by Hspice simulation as shown in Fig. 4(b).

Secondly, we consider the delay for the falling transition. The resistance R_{n+1} degrades the value of V_n , so the capacitance C_L is discharged starting at a lower voltage $V_{dd} - \Delta V_n$. In another way, the breakdown resistance R_{n+1} can also discharge

the capacitance. Then the delay for the falling transition can be expressed by

$$\begin{aligned} t_{pf,n}^* &= - \int_{V_{dd} - \Delta V_n}^{V_{dd}/2} \frac{C_L}{I_{dsatn,n} + V/R_{n+1}} dV \\ &\approx \frac{C_L V_{dd}}{2I_{dsatn,n}} \left(1 - \frac{2\Delta V_n}{V_{dd}}\right) \left(1 - \frac{\Delta V_n}{4V_{dsatn}}\right) \\ &\approx \frac{C_L V_{dd}}{2I_{dsatn,n}} \left(1 - \frac{2\Delta V_n}{V_{dd}} - \frac{\Delta V_n}{4V_{dsatn}}\right) \end{aligned} \quad (18)$$

Thus the delay variation is given that

$$\Delta t_{pf,n} = - \left(\frac{2\Delta V_n}{V_{dd}} + \frac{\Delta V_n}{4V_{dsatn}} \right) t_{pf,n} \quad (19)$$

It should be noticed that Eq. (19) shows that TDDB can lead to the delay reduction which is verified by Hspice simulation as shown in Fig. 4(c).

Finally, for INV_n , the delay variation for the rising transition can be calculated by Eq. (17) directly, while the delay variation for the falling transition should be combined by Eq. (12) and (19). It is given that

$$\Delta t_{pf,n} = \left(\frac{\Delta V_{n-1} - 2\Delta V_n}{V_{dd}} - \frac{\Delta V_n}{4V_{dsatn}} \right) t_{pf,n} \quad (20)$$

C. Delay model considering both TDDB and NBTI

The NBTI effect degrades the threshold voltage of pMOS transistor, and thus the charging current at the rising transition. The saturation current is given that

$$I_{dsatp,n} = v_{satp} C_{oxp} W (V_{dd} - V_{thp,n} - \Delta V_{thp,n} - \frac{V_{dsatp}}{2}) \quad (21)$$

Thus we can get the increase of the delay for the rising transition

$$\Delta t_{pr,n} = \frac{\Delta V_{thp,n} \cdot t_{pr,n}}{V_{dd} - V_{thp,n} - V_{dsatp}/2} \quad (22)$$

Therefore, if we consider both TDDB and NBTI, the delay variation for the rising transition should be

$$\Delta t_{pr,n} = \left(\frac{\Delta V_{thp,n}}{V_{dd} - V_{thp,n} - V_{dsatp}/2} + \frac{\Delta V_n}{4V_{dsatp}} \right) t_{pr,n} \quad (23)$$

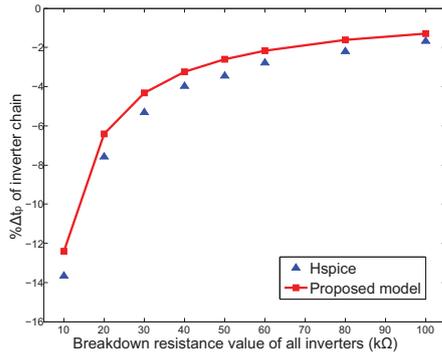


Fig. 5. Degradation of voltage swing due to the breakdown resistance

Meanwhile, the delay variation for the falling transition can be estimated still using Eq. (20).

This analytical model can be integrated into STA tools as follows. As mentioned in Section III-A, the node degradation can be calculated by characterizing each type of logic gate in a technology library, and then the delay variation of each node in the signal path can be estimated by Eq. (20) and (23).

D. Model validation for inverter chain

Delay analysis has been applied to an inverter chain and shown in Fig. 3. Assuming that all the inverters have the same size and are symmetrically designed, the delay of the inverter chain is

$$t_p = \frac{N}{2}(t_{pr,n} + t_{pf,n}) = Nt_{p,n} \quad (24)$$

where N is the stage number of the inverter chain.

We assume that all the breakdown resistances have the same value, thus ΔV_n are the same for all the nodes. Therefore,

$$\begin{aligned} \Delta t_p &= \frac{N}{2} \left[\frac{\Delta V_n}{4V_{dsatp}} t_{pr,n} - \left(\frac{\Delta V_n}{V_{dd}} + \frac{\Delta V_n}{4V_{dsatn}} \right) t_{pf,n} \right] \\ &\approx -\frac{Nt_{p,n}}{2} \cdot \frac{\Delta V_n}{V_{dd}} = -\frac{\Delta V_n}{2V_{dd}} t_p \end{aligned} \quad (25)$$

The results can be verified by the Hspice simulation, as shown in Fig. 5. The inverter is constructed by the PTM 45nm bulk CMOS model [31]. The values estimated by our proposed model are slightly smaller than the simulated ones, but our proposed model shows the same trend as Hspice simulation. The trend shows an interesting phenomenon that the propagation delay may reduce as the TDDB effect becomes worse, which means the circuit may work faster.

If the NBTI effect is considered, our proposed model also shows a consistency with the Hspice simulation. We set all the pMOS devices to the same ΔV_{th} , and make similar verifications. The points and line in the above of Fig. 6 represent the regime of $\Delta V_{th} = 50\text{mV}$, and the below ones represent that $\Delta V_{th} = 10\text{mV}$. Fig. 6 shows that our model can predict the circuit delay due to TDDB and NBTI.

IV. DELAY VARIATION ANALYSIS FOR CIRCUITS

In this section, the 9-stage inverter chain is used as our benchmark, and it is constructed using the PTM 45nm bulk

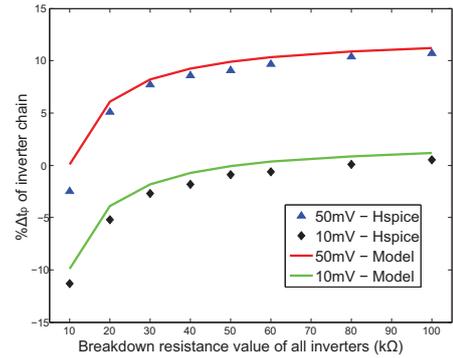


Fig. 6. Degradation of voltage swing due to the breakdown resistance

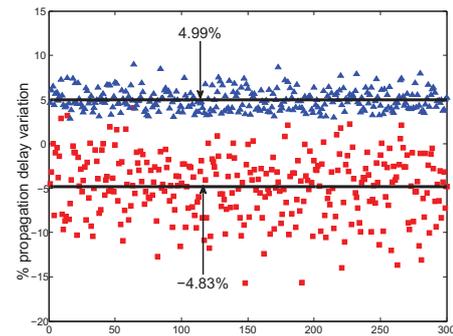


Fig. 7. Delay variation compared with no output degradation

CMOS model [31]. Similar approaches can be applied to more complex combinational circuits, since each signal path acts similarly as the inverter chain.

A. Comparison between w and w/o output degradation

If the degradation of the output nodes in the logic gates is not considered in delay evaluation, as presented in [15], the delay variation can be estimated incorrectly.

As shown in Fig. 7, the triangle symbols above in the figure represent the simulated results using the delay model in [15], while the square symbols below in the figure represent the results using our models. In both simulation, R_{BD} is randomly chosen in $10\text{k}\Omega$ to $50\text{k}\Omega$.

Fig. 7 shows the model in [15] predicts the average delay variation of 5.0% , while our model predicts the average of -4.8% . The difference is almost 10% of total circuit delay, and the trend of this variation is reversed. Thus, considering with or without the output degradation can make a great difference to the overall circuit delay.

B. Spatial correlation analysis

In this section, the spatial correlation of TDDB effect, which means the location of the breakdown gate in the signal path, will be investigated.

1) *Case of one breakdown inverter*: It is assumed that only one inverter in the chain gets distinct breakdown. This inverter is denoted as the “breakdown inverter”. The value of R_{BD} of the breakdown inverter varies from $10\text{k}\Omega$ to $15\text{k}\Omega$, and others have the value from $100\text{k}\Omega$ to $500\text{k}\Omega$, which means these

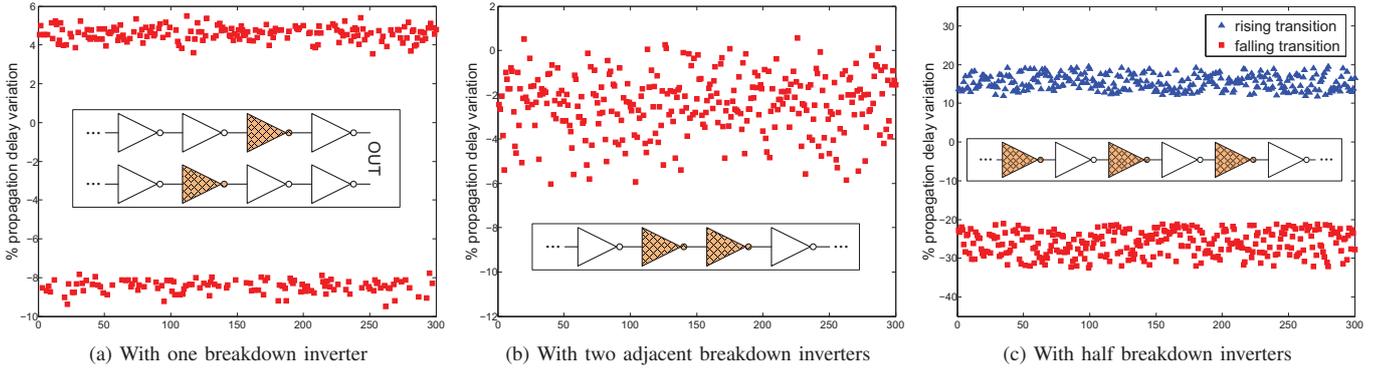


Fig. 8. Spatial correlation analysis of TDDB effect

inverters only get slightly breakdown. The breakdown inverter is randomly selected in our simulation. The breakdown gate is shaded in the schematic of Fig. 8(a).

The results are shown in Fig. 8(a). It is very interesting that the delay variation is bipolar, and shows about 13% difference in circuit delay. The breakdown inverter located in some places may degrade the delay, but it can boost the circuit in other places. This phenomenon can be explained by our TDDB model. As shown in Fig. 3, if INV_n is the breakdown inverter, the degradation of V_{n-1} can affect two inverters INV_n and INV_{n-1} .

For INV_n , from Eq. (12), the delay for the falling transition degrades by the following equation

$$\Delta t_{pf,n} = \frac{\Delta V_{n-1} \cdot t_{pf,n}}{V_{dd}} \quad (26)$$

For INV_{n-1} , the delay variation for the rising transition can be derived from Eq. (17)

$$\Delta t_{pr,n-1} = \frac{\Delta V_{n-1} \cdot t_{pr,n-1}}{4V_{dsatp}} \quad (27)$$

The delay variation for the falling transition is derived from Eq. (19)

$$\Delta t_{pf,n-1} = - \left(\frac{2\Delta V_{n-1}}{V_{dd}} + \frac{\Delta V_{n-1}}{4V_{dsatn}} \right) t_{pf,n-1} \quad (28)$$

Depending on the location of the breakdown inverter INV_n in the chain, the delay variation $\Delta t_1 = \Delta t_{pf,n} + \Delta t_{pr,n-1}$ may contribute to the delay for the rising transition, while $\Delta t_2 = \Delta t_{pf,n-1}$ contributes to the delay for the falling transition, and vice versa. As the example circuit schematic shown in Fig. 8(a), in the above schematic, the delay variation Δt_1 contributes to the rising transition of the output node, while the delay variation Δt_2 contributes to the falling transition. In the below schematic, Δt_1 contributes to the falling transition, while Δt_2 contributes to the rising transition. In brief, this phenomenon can be considered as the spatial correlation of the TDDB effect.

Besides, only the delay variation for the rising transition is shown in Fig. 8(a). Our analysis indicates the breakdown inverter makes the circuit to become very asymmetric. If the

delay for the rising transition is reduced, the delay for the falling transition will be increased, and vice versa.

2) *Case of two adjacent breakdown inverters:* In this case, two adjacent inverters are assumed to get breakdown. In our analysis, these two breakdown inverters are denoted as INV_n and INV_{n-1} . As shown in Fig. 3, R_n and R_{n-1} randomly vary in the region of $10k\Omega$ to $15k\Omega$. The simulated results in Fig. 8(b) show the mean value of the delay variation is -2.4% .

We can carry out the similar derivation as in the above, and verify the result. We assume the breakdown of INV_n can contribute the delay variation Δt_1 to the overall delay for the rising transition, and thus a negative Δt_2 contributes to the delay for the falling transition. Furthermore, the breakdown INV_{n-1} contributes the negative Δt_2 to the rising transition, while Δt_1 is contributed to the falling transition. The same derivation can be applied on the reverse assumption.

After all, $\Delta t_1 - \Delta t_2$ contributes to both the rising and falling transition, and the circuit remains temporal symmetrical. Depending on the value of Δt_1 and Δt_2 , the circuit performance may be degraded or boosted up.

According to the above analysis, we can conclude that if half inverters are distinct breakdown, and all these breakdown inverters are not adjacent (Fig. 8(c)), then the temporal characteristic will be very asymmetric. As shown in Fig. 8(c), the simulation shows the average delay variation for the rising transition is about 15%, while about -25% for the falling transition. The difference is about 40% in circuit delay.

3) *Case of ring oscillator:* If the inverter chain is ringed, this circuit will oscillate with a period

$$T_{osc} = \sum_i (t_{pr,i} + t_{pf,i}) \quad (29)$$

where $t_{pr,i}$ and $t_{pf,i}$ are the propagation delay of the inverter INV_i for the rising and falling transition, respectively. This equation means that both the delay for the rising and falling transition are considered in calculating the period.

Thus, in a ring oscillator, the absolute location of the inverter will not affect the oscillator period, because all the inverters in the ring are equal. We will consider two breakdown inverters with different relative locations.

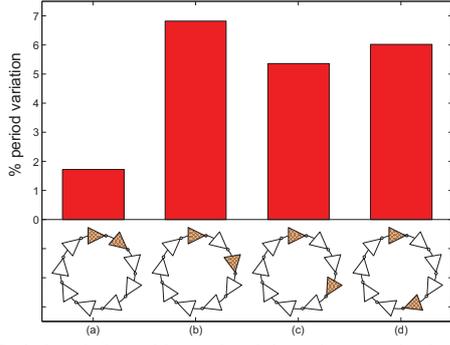


Fig. 9. Period variation with two breakdown inverters in ring oscillator

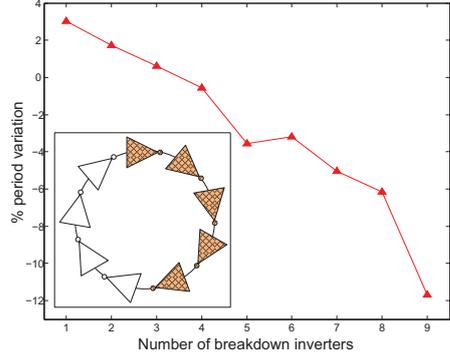


Fig. 10. Period variation with N breakdown inverters ($N = 1 \sim 9$)

As shown in Fig. 9, we use Hspice to simulate the period of the ring oscillator with two breakdown inverters. The ring has 9 stages of inverters, and there are four different possible locating modes of these two breakdown inverters. As shown in Fig. 9, mode (a) represents these two inverters are adjacent, while mode (b) to (d) correspond to they are separated by one to three fresh inverters, respectively. The simulation shows the period of the ring oscillator varies 1.7%, in mode (a), and in mode (b) to (d), the variations are 6.8%, 5.4% and 6.0%. In mode (a), these two breakdown inverters have very strong spatial correlation, but in other modes, they are weakly correlative. Therefore, the variation in mode (a) is very different with in other modes.

From the simulation results in Fig. 9, we can guess the two adjacent breakdown inverters can reduce the performance degradation due to TDDB, and may boost up the circuit. Fig. 10 shows the simulation results comparing the period variation with 1 to 9 breakdown inverters, and all these inverters are adjacent. The results show the ring oscillator can have higher oscillator frequency with more breakdown inverters. When all 9 inverters get breakdown, the oscillator can boost up with about 12%. We get that TDDB effect may boost up the circuit by now.

C. Delay analysis considering both TDDB and NBTI

Firstly, it is assumed that the TDDB and NBTI affects all the inverters randomly, which means the degradation of the threshold voltage ΔV_{th} and the breakdown resistance R_{BD} at each input node is randomly selected.

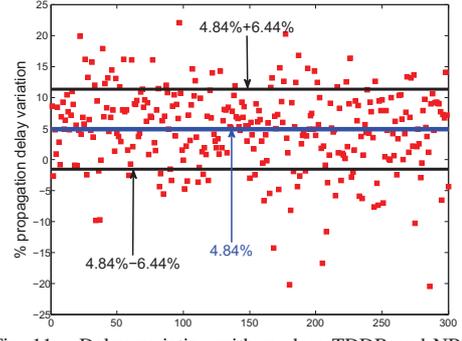


Fig. 11. Delay variation with random TDDB and NBTI

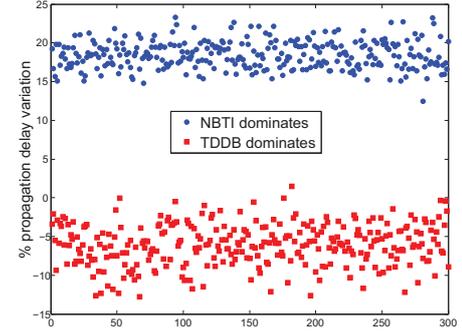


Fig. 12. Delay variation with TDDB and NBTI dominating respectively

In this analysis, ΔV_{th} is assumed to vary from 10mV to 60mV, R_{BD} varies from 10k Ω to 150k Ω . The Monte-Carlo analysis is applied on the inverter chain, and the results are shown in Fig. 11. The mean value of delay variation is 4.8%, and this mean value is represented by the middle line in Fig. 11. Meanwhile, the standard deviation is 6.4%, and this value is indicated by the above and below lines.

The results show the delay variation can be very randomly, because the TDDB affects the circuit delay very complicatedly. The detail will be described in the following.

Secondly, two cases are considered:

- Case A: The NBTI effect dominates in the inverter chain, thus ΔV_{th} varies from 50mV to 100mV. In addition, the breakdown resistance R_{BD} is chosen from 100k Ω to 500k Ω .
- Case B: In contrast with Case A, the TDDB effect dominates in this case, and R_{BD} varies from 10k Ω to 30k Ω , while ΔV_{th} from 0mV to 20mV.

The results are shown in Fig. 12. In Case A, the mean value of delay variation is 18.5%, and the standard deviation is 1.8%. In Case B, the mean value is -6.1% , and the standard deviation is 2.7%. The results show the NBTI effect always degrades the circuit performance, but TDDB effect may boost the circuit.

Furthermore, Fig. 13 shows NBTI effect degrades the circuit delay continuously. In this analysis, R_{BD} varies from 10k Ω to 150k Ω . The mean value of delay variation can be less than 0 with ΔV_{th} in the region of 0~10mV, but this value can be reach up to 14% within the region of 60~70mV. The standard deviation is almost constant as shown in Fig. 13.

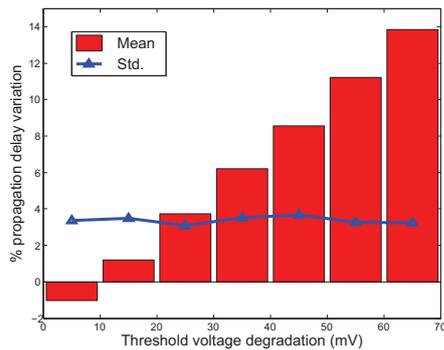


Fig. 13. NBTI degrades circuit delay

V. CONCLUSION

This paper considers the output degradation of the breakdown gates in evaluating the temporal performance of digital circuits. Compared with the analysis without considering this factor, the difference can be 10% of the total circuit delay in average. The spatial correlation of TDDB effect is demonstrated in this paper, and up to 40% difference in circuit delay can be observed depending on the location of the breakdown gate in the signal path. Both TDDB and NBTI are considered in our proposed model, which shows that NBTI always degrades the circuit performance, but TDDB may boost up the circuit. Our proposed model can be integrated into STA tools and current design flows.

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