Three-Dimensional Integrated Circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis

Paul Falkenstern and Yuan Xie
Pennsylvania State University
Computer Science and Engr. Dept.
University Park, PA, USA

Yao-Wen Chang
National Taiwan University
Dept. of Electrical Engr.
Taipei, Taiwan

Yu Wang
Tsinghua University
TNlist, Dept. of Elec. Engr.
Beijing, China

Abstract— **Three Dimensional Integrated Circuits (3D ICs) are currently being developed to improve existing 2D designs by providing smaller chip areas and higher performance and lower power consumption. However, before 3D ICs become a viable technology, the 3D design space needs to be fully explored and 3D EDA tools need to be developed. To help explore the 3D design space and help fill the need for 3D EDA tools, the 3D Floorplan and Power/Ground (P/G) Co-synthesis tool is developed in this work, which develops the floorplan and the P/G network concurrently. Most current 3D IC floorplanners neglect the effects of the 3D P/G network on the design, which may lead to large IR drops in the circuit. To create feasible floorplans with efficient P/G networks, the 3D Floorplan and P/G Co-synthesis tool optimizes the floorplan in terms of wirelength, area and P/G routing area and IR drops. The tool integrates a 3D B*-tree floorplan representation, a resistive P/G mesh, and a Simulated Annealing (SA) engine to explore the 3D floorplan and P/G network. The results of experiments using the 3D Floorplan and P/G Co-synthesis tool show that 3D ICs tend to increase the P/G routing area while decreasing the IR drops in the circuit. By considering the IR drop while floorplanning, exploring the 3D P/G design space, and evaluating 3D IC's effect on 3D P/G networks, the 3D Floorplan and P/G Co-synthesis tool can develop a more efficient 3D IC.**

I. Introduction

Today's integrated circuit technology continues to scale to smaller feature sizes, improving the performance of gates. However, because global interconnects do not scale accordingly with technologies, they have become a major performance and power bottleneck [1]. As technology scales, solutions are needed that can overcome the limitations of wiring requirements for present and future chip designs.

Three-dimensional integrated circuits (3D ICs) [2] offer an attractive solution for overcoming the barriers to interconnect scaling, thereby offering an opportunity to continue performance improvements using CMOS technology, with smaller form factor, higher integration density, and the support for the realization of mixed-technology chips. Among several 3D integration technologies [3], TSV (Through-Silicon-Via) approach is the most promising one and therefore is the focus of the majority of 3D integration R&D activities [1]. A TSV-based 3D chip consists of multiple device layers stacked together with direct vertical interconnects (through-silicon vias, or TSVs) tunneling through them.

Even though manufacture/process techniques for 3D integrations are nearly mature [1], [4], and 3D ICs offer tremendous benefits, one of the challenges that hinder the successful adoption of 3D technology is the lack of commercially available electronic design automation (EDA) tools and design methodologies for 3D ICs [5]. The absence of EDA tools that can explore the design space is an impediment to researchers and industry practitioners in their quest for the adoption of this new technology. Consequently, there are many R&D activities on developing EDA tools and methodologies tailored specifically for 3D IC designs.

3D IC design is fundamentally related to the topological arrangement of logic blocks. Therefore, physical design tools for 3D circuits are important for the adoption of 3D technology [6]–[9]. Among various physical design problems, floorplanning and power/ground(P/G) network synthesis both play an important role in the early stages of the IC design flow:

- The floorplanning stage defines the placement of the major blocks and components of the IC, affecting the optimization results of the subsequent stages including placement and routing.
- P/G network synthesis sizes and places the power and ground lines for the chip. There are two important optimization goals for P/G network synthesis: (1) *Minimize IR drop*, which can have negative impact on the performance of the circuit. IR drop has become more important as technology scales, because as the wires shrink with smaller feature sizes, the resistances along the power lines increase. (2) *Minimize the routing area* of the P/G wires, which causes congestion during later routing stages. However, there is potential conflict between these two optimization goals. For example, using wider wires for P/G network could help reduce IR drop but the routing area is increased. Consequently, a design tradeoff between the P/G area and IR drop is needed.

Even though there exist studies on 3D IC floorplanning, most do not consider the P/G delivery to the blocks. On the other hand, there has been little research on 3D P/G networks. To help explore the 3D design space and help fill the need for 3D EDA tools, in this work, we develop a 3D floorplan and P/G co-synthesis tool. To the best of our knowledge, this is the first work that combine 3D floorplanning and P/G network synthesis together.

The rest of the paper is organized as follows: Section II presents the motivation and related work. Section III formulates the 3D Floorplan and P/G Co-synthesis problem and Section IV describes the algorithm for Co-synthesis. Section V presents experimental results using the Co-synthesis tool. Finally, a conclusion is given in Section VI.

II. Motivation and Related Work

In this section, we first discuss the motivation of our work, and the present the related work.

A. Why 3D Floorplan and P/G Network Co-Synthesis is Needed

In a traditional design flow, floorplanning and P/G network design are two sequential steps: the floorplanning is performed first to optimize chip area and wire length, and then the P/G network is synthesized. However, it has been shown by Liu and Chang [10] that, in 2D IC design, if the floorplan does not consider the P/G network, the resulting floorplan may lead to an inefficient P/G network with high IR drops and several P/G voltage violations. It is very difficult to repair a P/G network after the post-layout stage, so the P/G network should be considered as early as possible. Consequently, Liu and Chang proposed a floorplan and P/G network co-synthesis method to efficiently solve the problem [10].

In Floorplan and P/G co-synthesis, the P/G network is created during floorplanning. During co-synthesis, the floorplan not only tries to minimize the wirelength and area of the design, but also ensures that there are no power violations to the blocks in the floorplan. This

978-1-4244-5767-0/10/$26.00 2010 IEEE

results in a floorplan with an efficient P/G network. *However, existing research on floorplan and P/G co-synthesis only supports 2D ICs and is not extended to 3D ICs.*

B. Related Work

Related work to this project includes prior research in developing 3D EDA tools for floorplanning and Power/Ground (P/G) network designs.

- **3D Floorplanning:** We have seen recent research in creating new 3D EDA tools such as floorplanners, placers and routers [6], [8], [9]. For 3D floorplanning, Hung et al. has proposed a 3D-IC floorplanner that considers thermal impact [11]. The Combined Bucket Array consists of a 2D representation for each tier and a bucket structure that stores the vertical relationship of blocks [12]. Also, the Transitive Closure Graph (TCG) was extended to support 3D ICs with Layered-TCG (LTCG) [13]. However, when optimizing the floorplan, current 3D floorplanning tools mainly consider the 3D IC's wirelength, area and temperature, but usually neglect the P/G network.
- **3D Power/Ground Network Design:** Only a few works have explored 3D P/G construction. Decoupling capacitors (decaps) can be used during placement to reduce the power supply noise [14], [15]. In these works, the resistive and inductive effects of a 3D P/G grid were used to calculate the decap budget for each placed module. Considering decaps during placement reduced the total number of decaps needed to adequately reduce the power supply noise [16]. In addition to using decaps to reduce P/G noise, the density of P/G TSVs can be adjusted to reduce the power supply noise [17]. However, the existing works on the P/G network do not completely adjust the characteristics (size and pitch) of the 3D P/G network, or consider different P/G topologies. Therefore, the 3D P/G design space is not fully explored. In addition, the effects of the 3D floorplanning on the P/G metrics are not completely presented.

III. Problem Formulation

The 3D Floorplanning and P/G Co-synthesis problem can be formulated as follows: *Given the module information of a design, the current consumed by each module, a netlist connecting the modules, pre-placed I/O pads, and the number of tiers T, construct a feasible floorplan and P/G network for the design which minimizes the area, wirelength, P/G routing area and IR drop of the 3D IC.*

The module information of the design is a set of m modules. Each module has width and height dimensions, as well as a set of pins. The netlist of the design connects the pins of the various modules and the I/O pads. One of the nets is indicated as the power net, and another net is indicated as the ground net. Each pin of a module in a power or ground net, p_i, has an associated current, I_i, which it consumes. For power pins, this value is positive indicating current flowing into the module, and for ground pins this value is negative indicating current flowing out of the module.

The floorplan, F, describes the 3D placement and rotation for each module. For each module m_j, its placement is (x_j, y_j, t_j, r_j), where x_j is the x-coordinate, y_j is the y-coordinate, t_j is the tier, and r_j is the rotation of m_j. Once all the modules are placed, the chip's Area, A, and Wirlength W can be determined.

A P/G network can be described by a graph $G = (N, E)$ with n nodes ($N = n_1, n_2, \ldots, n_n$ and e edges $E = e_1.e_2, \ldots, e_m$. Each node $n_i, 1 \leq i \leq v$ has a 3D location (x_i, y_i, t_i). Each edge $e_i, 1 \leq i \leq e$ connects two nodes n_j and $n_k, 1 \leq j, k \leq v$. The P/G Network must meet several power integrity constraints: the IR drop constraint, the minimum width constraint, and the electromigration constraint. These constraints are described below.

- **IR-drop Constraint:** For every P/G pin pin_j in a module, its corresponding voltage of V_j must satisfy the following constraints:
  $V_j \geq V_{min}$ if pin_j is a power pin
  $V_j \leq V_{max}$ if pin_j is a ground pin
  where $V_{min}(V_{max})$ is the minimum (maximum) required supply voltage for power (ground) pins in the circuit. This constraint ensures that the chip the modules with enough power to function correctly and with an acceptable performance.
- **Minimum Wire Width Constraint:** For every P/G edge e_i in the P/G Network G, its width is greater than the minimum width allowed on the wire layer in the technology:
  $w_i \geq w_{min}$, where w_i is the width of e_i and w_{min} is the minimum width allowed.
- **Electromigration Constraint** For every P/G edge ,e_i, must meet an electromigration constraint:
  $I_i/w_i \leq \sigma$
  where σ is a an elecgromigration constant for the metal layer of the edge. This is to provide an upper bound to the current density in the edge to ensure the wires do not break down.

To compare the quality of P/G Networks in delivering supply voltages, a P/G penalty (Φ) can be calculated for the P/G Network in a floorplan. The penalty considers any electromigration violations, and any IR-drop violations, as well as the value of the IR-drop at each pin. For pin pin_j with a voltage of V_j, the IR-drop is:

$$ir_j = \begin{cases} V_{in} - V_j & \text{if } pin_j \text{ is a power pin} \\ V_j & \text{if } pin_j \text{ is a ground pin} \end{cases}$$

where V_{in} is the input voltage of the power supply.
The P/G Network penalty can then be calculated as follows:

$$\Phi(G) = \eta * e_{em}/e + \theta * p_v/p + \kappa * ir_{avg} + \lambda * ir_{max} \quad (1)$$

where G is the P/G network, η, θ, κ and λ are weight factors, e_{em}/e is the ratio of branches with electromigration constraint violations, p_v/p is the ratio of power/ground pins with voltage drop violations, ir_{avg} is the average IR-drop of all power/ground pins, and ir_{max} is the maximum IR-drop of all power/ground pins.

The objective of Floorplan and P/G Co-synthesis is to find a solution of the floorplan and P/G network that balances the wirelength between the modules, the total area of the chip, the P/G routing area and the P/G IR drop. This can be done by calculating a cost(Ψ) for each floorplan (F):

$$\Psi(F) = \alpha * A + \beta * W + \gamma * Dev + \epsilon * \Phi + \zeta * PG_{area} \quad (2)$$

where $\alpha, \beta, \gamma, \epsilon$ and ζ are weight parameters; A is the area of the 3D IC, calculated by multiplying the width of the tier with the largest width by the height of the tier with the largest height; W is the wirelength between the floorplan blocks; Dev is the sum of the difference of the height and width of each tier with the average width and height of the tier and is used to balance the dimensions of each tier; Φ is the total penalty of the P/G network, and PG_{area} is the routing area of the P/G network.

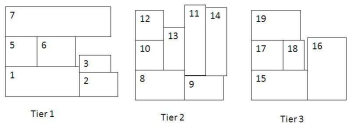
IV. 3D Floorplan and P/G Co-synthesis Algorithm

In our work, the 3D floorplan and power/ground co-synthesis tool is developed by integrating a 3D B*-tree floorplan representation, a resistive P/G mesh, and a Simulated Annealing (SA) engine. The

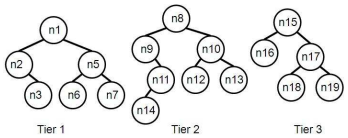
tool allows 3D ICs to optimize the floorplan in terms of wirelength, floorplan area, P/G routing area, and IR drops. In addition, the tool will permit the exploration of different P/G network methodologies on 3D ICs. Two different P/G mesh topologies are analyzed: a uniform mesh with the same mesh for each tier and a non-uniform mesh with different sized meshes for each tier. The co-synthesis algorithm can also examine how the 3D IC affects the P/G routing area and the IR drop of the circuit, which will allow an efficient 3D P/G network design that balances each P/G metric. By exploring the properties of 3D P/G networks, the effect of 3D ICs on P/G networks can be analyzed, giving a more complete understanding of the benefits and limitations of 3D ICs.

A. 3D B*-Tree Floorplan Representation

The representation for the floorplan used in the 3D Floorplan and P/G Co-synthesis algorithm is the 3D B*-trees, In the 3D B*-tree representation, a B*-tree is used to represent the floorplan in each tier. The B*-tree, a 2D floorplan developed by Chang *et al.* [18], is an ordered binary tree that has a unique correspondence to a compacted floorplan. In 3D B*-tree (Fig. 1), a B*-tree is used for each tier of the 3D IC. The modules in a tier's B*-tree are placed on that tier with the 2D placement of the B*-tree.



(a) An Example 3D IC Floorplan



(b) 3D B*-tree of Floorplan

Fig. 1. 3D B*-tree Floorplan Representation

To explore the 3D floorplan solution space, the 3D B*-trees can be modified in the following ways:

- 1. Node swap, which swaps two modules in the same B*-tree
- 2. Rotation, which rotates a module
- 3. Move, which moves a module to a different location in the same B*-tree
- 4. Inter-tier swap, which swaps two modules at different tiers
- 5. Inter-tier move, which moves a module to a different tier

The first three perturbations are the original perturbations of a B*-tree [18]. These perturbations only change a single B*-tree and thus modify the floorplan of only one tier. The last two perturbations are introduced specifically for 3D floorplanning. Because the original perturbations only modified the floorplan in the 2D space, the inter-tier perturbations are created to explore the 3D design space of the floorplan. By using these perturbations, different floorplans can be modeled, analyzed and compared.

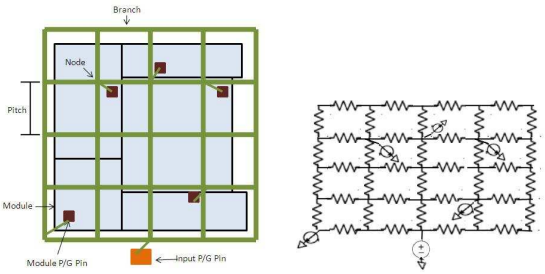
A popular method to explore the solutions space of the floorplan representations is to use simulated annealing (SA) [19], [20]. At each step of SA, the current floorplan F is perturbed to a new floorplan, F'. If F' has a lower cost than F, then F' becomes the current floorplan. If the cost of F' is higher than F, F' becomes the current floorplan with a small probability, which is dependent on the difference of the costs and a variable called temperature $Temp$. A high temperature is initially selected, but as SA progresses, the temperature decreases to limit the selection of worse floorplans. The process of perturbing the floorplan is continued until a certain point where the floorplan is considered near optimal. The floorplan with the lowest

The SA engine used in this work consists of two stages. The first stage consists of floorplan perturbations involving the whole 3D floorplan; during the second stage only floorplan perturbations on a single tier are performed. In the first stage, the floorplan moves consist of either moving or rotating a block in its tier, or moving or swapping blocks between tiers. In the second stage, a single tier is picked, and a block is moved or rotated within that tier. There are two stages because the first stage attempts to find the best partition of the blocks into separate tiers. However, because blocks are moved from tier to tier, each individual tier may not be optimized. Thus the second stage tries to optimize each tier.

B. P/G Synthesis

The P/G Network created in this project is based on the mesh structure (or grid), as shown in Figure 2(a). The pitch of the grid determines the distance between each power/ground line. In representing the P/G network as a graph, each intersection of the P/G wires is considered a node in the graph. To decrease the complexity of P/G analysis, each power and ground pin of the floorplan block is connected to the closest P/G node. Each power pin in the IC will consume a given amount of current at the given node. Each power pin from the IO pad will supply the network node with the supply or ground voltages. The module's P/G pins and the IO pins connect to the nodes in the P/G mesh.

Once the P/G network is created from the floorplan and pitch, it needs to be analyzed by calculating all the voltages at the nodes and pins, as well as checking electromigration constraints. In this work, static P/G methods are used to achieve a fast analysis of the P/G network. More sophisticated P/G network simulation techniques may be too time-consuming for co-synthesis in the early design stages. Therefore, the P/G networks are analyzed using a resistive model, where the branches are replaced with resistances. Figure 2(b) shows a resistive model of the P/G mesh from Figure 2(a) The resistance of edge $edge_i$ is calculated by $R_i = \frac{r_{sq} * l_i}{w_i}$, where r_{sq} is the sheet resistivity of the material of the edge, l_i is the length of the edge and w_i is the width of the edge.



(a) Example P/G Mesh Network (b) Resistive P/G Model

Fig. 2. P/G Mesh and Resistive Model

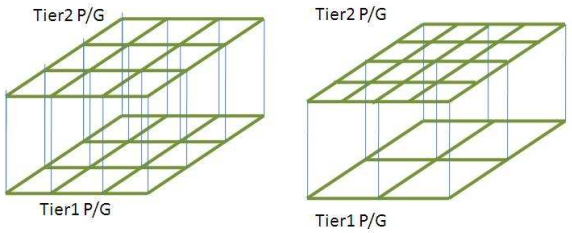
Modified Nodal Analysis (MNA) is used to analyze the P/G network. MNA solves $\mathbf{Gx} = \mathbf{i}$, where $\mathbf{G}$ is the conductance matrix (the conductance of $edge_i$ is $G_i = \frac{1}{R_i}$) of the mesh, containing all the conductance information of each branch of the mesh; $\mathbf{x}$ is a vector containing all the unknown voltages of the nodes; and $\mathbf{i}$ is a vector containing all the currents consumed by the nodes, as determined when placing each pin to a node. $\mathbf{Gx} = \mathbf{i}$ can be solved using linear algebra techniques. Once all the voltages for

the nodes are known, then the voltages supplied to the pins can be determined. For a P/G pin in a module, pin_j, its voltage is calculated by $V_j = V_{node} - \frac{I_j * d * r_{sg}}{w}$, where V_{node} is the voltage of the node connected to the pin, d is the distance between the pin and the node, w is the width of the strap connecting the pin and the node. Once all the voltages for the nodes and pins are known, the various constraints can be checked, and the P/G penalty Φ can be calculated.

A P/G Mesh can be constructed for 3D ICs to supply power by using a global mesh, where there is one P/G network for the entire chip. Each tier has its own 2D P/G mesh, and each tier's 2D mesh is connected using TSVs. These TSVs are also represented by edges in the P/G network. In this work, two methods are used to construct the global mesh: a uniform mesh and a non-uniform mesh.

In a uniform mesh (Figure 3(a)), the pitch of each tier's 2D mesh is equal. This pitch can be adjusted by the algorithm to control the properties of the P/G network. In the SA algorithm, the pitch from the previous floorplan F is adjusted to create a pitch for the new floorplan F'. If the previous floorplan has any IR drop or electromigration violations, then the pitch is decreased. If there are no violations, then the pitch either increases, decreases or stays the same, all with the same probability of 33%.

In a non-uniform mesh (Figure 3(b)), the 2D meshes for each tier could have a different pitch. Each tier's pitch can be adjusted individually to control the P/G network. Thus, a non-uniform mesh may balance the P/G area and IR drops in the circuit more efficiently. To update the pitch for each tier from F to F' in the SA algorithm, a tier penalty for each tier is calculated. The tier penalty is calculated from the electromigration violations, voltage drop violations, average voltage drops and maximum voltage drops occurring on the pins on that tier. The pitch for each tier is updated with the same strategy as a global pitch. If a violation occurs on a tier, then that tier's pitch is decreased. If there are no violations in the tier, then the tier's pitch either increases, decreases or stays the same, again all with a probability of 33%.



(a) 3D Uniform P/G Mesh (b) 3D Non-uniform P/G Mesh

Fig. 3. 3D Uniform and Non-uniform P/G Mesh

TSVs are used to connect the 2D meshes of each tier for both the uniform and non-uniform 3D mesh. In this work, a TSV is constructed between two adjacent tiers when both tiers have nodes aligned with the same (x,y) location. In addition, a P/G TSV interval (i_{TSV}) controls the interval of aligned nodes that are connected with a TSV. In the uniform mesh, the TSV interval is adjusted because every node is aligned, and there may be many TSVs in the P/G mesh. In the non-uniform mesh, because nodes in adjacent tiers may not be aligned, the TSV interval is set to 1.

C. Algorithm and Design Flow

The methods above describe how to represent the 3D floorplan and construct the P/G network for 3D ICs. The 3D Floorplan and Co-synthesis algorithm (Figure 4) integrates to produce a floorplan and P/G network that consider the design metrics of chip area, wirelength, P/G routing area and P/G IR drops.

The algorithm starts by receiving the design information, which includes the module information, the initial P/G pitch and the P/G constraints. After an initial floorplan F is created and saved as the best floorplan F_{best}, the first stage of SA starts. In each iteration of the first stage of SA, the floorplan is perturbed with one of the five 3D B*-tree perturbations and a new P/G pitch is calculated, creating the new floorplan F'. The cost of the new floorplan, $\Psi(F')$ is computed. The new floorplan replaces the current floorplan according to the policies described by the SA process. It also replaces the best floorplan if $\Psi(F') < \Psi(F_{best}$.

After the first stage of SA, the second SA stage begins. The second SA stage is the same as the first stage, except that only the floorplan on one tier is perturbed. A random tier is selected, and one of the first three perturbations (Node swap, Rotate, or Move) is applied to the B*-tree of that tier. Once the second SA stage is complete, the algorithm returns the best floorplan F_{best}. It also returns the cost of the floorplan, the wirelength, area, P/G routing area, and P/G voltage drops.

The 3D Floorplan and P/G Co-synthesis algorithm can be inserted into an overall 3D design flow (Figure 5). Once the netlist has been synthesized and contains floorplan modules, these modules and the P/G constraints are taken as inputs for the 3D Floorplan and P/G Co-synthesis algorithm. The algorithm will return a floorplan and a P/G network which are used in the placement, routing and verification of the design. The P/G network can be further optimized in later stages of the design using more sophisticated and dynamic P/G analysis.

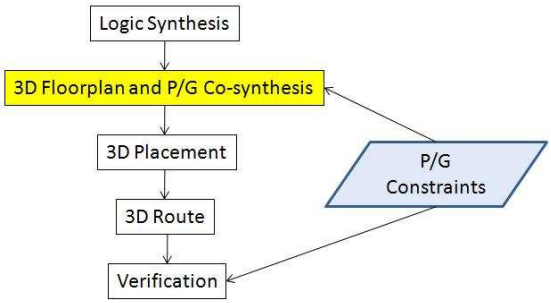


Fig. 5. 3D Design Flow with Floorplan and P/G Co-synthesis

V. Experimental Results

Experiments were conducted on the 3D Floorplan and P/G Co-synthesis algorithm using three MCNC floorplan benchmark circuits. The number of tiers in the 3D IC varied from 1 to 4 for each circuit. When the tier number was more than one, experiments for both uniform and non-uniform meshes were conducted. This section reports the results for the floorplan and P/G co-synthesis for uniform meshes and for non-uniform meshes.

Technology specifications and weighting factors in the P/G penalty and overall cost function must be set for the experiments. The input voltage was set to 1V ($V_{in} = 1$), and the minimum power voltage and maximum ground voltage was set to 15% of the input voltage. Thus $V_{min} = .85V$ and $V_{max} = .15V$. For the P/G network, the width of the P/G edges between P/G nodes was set to 30 μm, the sheet resistivity of horizontal P/G rails was set to .095 and the sheet resistivity of the vertical P/G rails was set to 0.055. The TSV distance was set to $50\mu m$ ($d_{TSV} = 50\mu m$) and the TSV width was set to $10\mu m$ ($s_{TSV} = 10\mu m$), and the TSV sheet resistivity was 0.055.

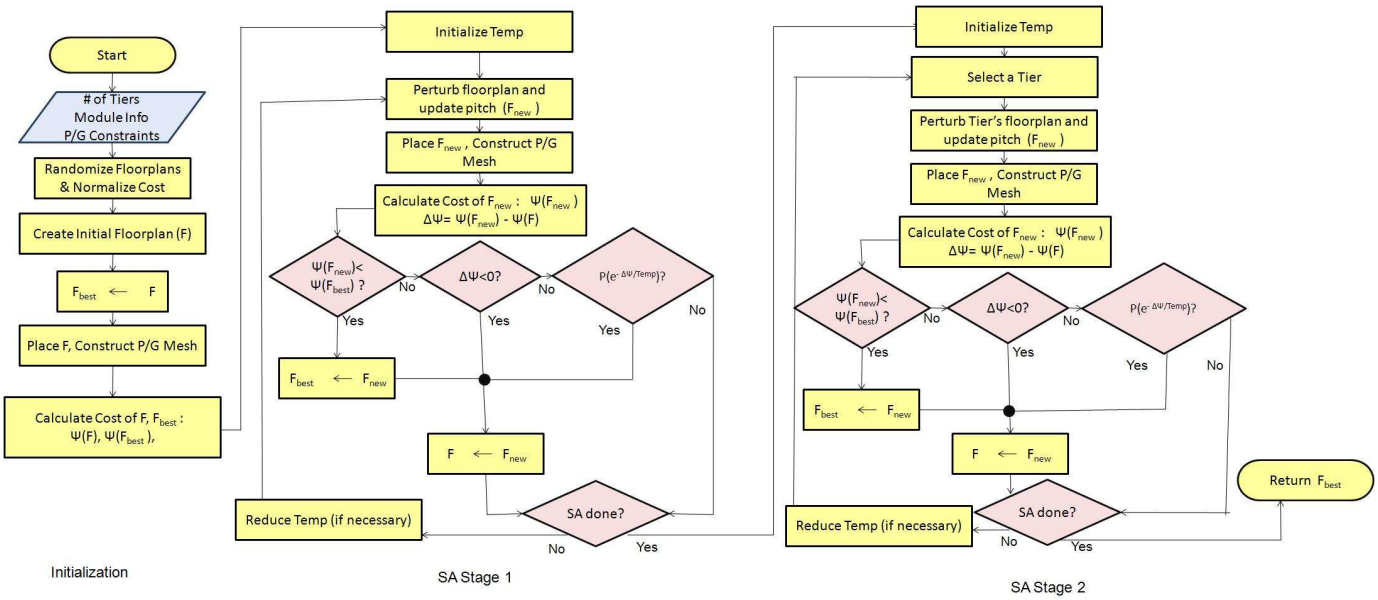


Fig. 4. 3D Floorplan and Power/Ground Co-synthesis Algorithm

Also, the width of the P/G straps from a node to a module's pins was set to $1\mu m$. The weights in the P/G penalty function were set to the following values: $\eta = 3, \theta = 7, \kappa = 1$ and $\lambda = 1$. Lastly, the weights of the algorithm's cost function was set to the following values: $\alpha = 0.3, \beta = 0.3, \gamma = 0.1, \epsilon = 0.025$ and $\zeta = 0.275$. Table I shows the results for the experiments with uniform meshes, while Table II shows the results for non-uniform meshes.

The results demonstrate that the area and wirelength decrease as the number of tiers increase, as expected and cited in previous works. These values decrease because 3D placement leads to higher packing densities and the decreased distance between modules. Also, the amount of dead space, which is the amount of area in the chip not occupied by a module, generally increases with the number of tiers due to the difficulty of equal packing distribution of the tiers. These results work validate the effects of 3D ICs on these circuit properties.

The experiments also show the resulting values of the P/G networks of the floorplans. First, the maximum IR drop shows that all of the pins receive an acceptable power or ground supply voltage. The maximum IR drop column indicates that all maximum IR drops are within $150mV$. This shows that the floorplanner can effectively create a P/G network which successfully supplies the circuit with the necessary voltage.

In addition, the results demonstrate important effects of 3D ICs on the P/G network properties. First, as the number of tiers increase, the total routing area of the 3D P/G network generally increases. The area the P/G network needs to cover is larger than the area of the chip because the stacked tiers allow higher packing densities. Because modules can be placed in each tier, the P/G mesh is also stacked throughout the chip in each tier. The area the P/G mesh consumes on each tier accumulates, resulting in a larger P/G routing area even though the area of the chip decreases and the modules are closer. A larger P/G routing area consumes wire space, increasing the challenges when routing the wires of the chip.

However, both the maximum and average IR drops of the 3D P/G networks generally decrease as the number of tiers increase in the circuit. Because the area of the chip is smaller and the modules are closer in the 3D design space, the P/G edges are shorter, similar to the global interconnects. The shorter P/G edges have less resistance, resulting in smaller IR drops in the P/G network. In addition, by placing modules in the 3D space, the current consumed by different modules may be diverted to different P/G edges in other tiers. Therefore, the individual 3D P/G edges have less current, which also results in smaller IR drops. Although 3D P/G networks are larger, they result in less IR drops. Because larger IR drops cause slower and even incorrect devices, smaller IR drops increase the performance of the circuit.

The average percent differences of the 3D P/G networks can be used to compare the two different topologies. The main difference between the two topologies is that the non-uniform mesh has a slightly better improvement in the average IR drop than the uniform meshes. This may be because separate pitches for each tier can more effectively deliver the power to the modules. In addition, for 3 tiers, the non-uniform mesh has a higher P/G routing area than the uniform mesh. However, there are no significant differences between the two types of meshes for the P/G area for 2 and 4 tiers and the maximum IR drop for all tiers. Though non-uniform meshes are more efficient in reducing the average IR drop in the circuit, both types of meshes have similar advantages and disadvantages.

These results show the effects of 3D ICs on the area, wirelength and dead space of a design, which have already been cited in previous studies. The results also demonstrate the effects of 3D ICs on the P/G network, leading to increased P/G area and decreased IR drops. These properties can aid in the designing of the 3D P/G network of the chip.

VI. Conclusion

A 3D Floorplan and P/G Co-synthesis tool was developed to create the 3D floorplan and the 3D P/G network simultaneously. The tool addresses the growing concern of IR drops in P/G networks for 3D ICs, while allowing for more effecting exploration of the 3D P/G design space. In addition, the experimental results shows the effect 3D ICs have on the P/G network. The P/G routing area increases while the IR drops decrease as the number of tiers increase. By considering the IR drop while floorplanning, exploring the 3D P/G design space,

TABLE I
UNIFORM MESH FLOORPLAN AND P/G CO-SYNTHESIS RESULTS

Circuit	Tiers	Area (um^2)	Deadspace (um^2)	Wirelength (um)	P/G Area (um)	Avg IR Drop (mV)	Max IR Drop (mv)	P/G Area vs 2D	Avg IR Drop vs 2D	Max IR Drop vs 2D
$ami33$	1	2144583	988133	183869	1392195	60.369	132.783	-	-	-
	2	1092982	1029514	130134	1755210	45.659	108.513	-26.08%	24.37%	18.28%
	3	927595	1626334	120520	2426625	44.527	97.779	-74.30%	26.24%	26.37%
	4	758018	1875621	109133	3103620	39.419	90.727	-122.93%	34.70%	31.67%
$apte$	1	59634951	13073323	841105	5978040	32.739	73.588	-	-	-
	2	32079783	17597938	639091	9669480	24.761	43.713	-61.75%	24.37%	40.60%
	3	21601316	18242320	552394	8907180	27.939	54.372	-49.00%	14.66%	26.11%
	4	15875922	16942060	459532	12778710	24.180	57.938	-113.76%	26.14%	21.27%
$xerox$	1	25717209	6366913	1085891	4919565	28.109	78.686	-	-	-
	2	13624879	7899462	766575	5726310	23.587	69.417	-16.40%	16.09%	11.78%
	3	9484354	9102767	616025	8118885	15.371	52.689	-65.03%	45.32%	33.04%
	4	6883398	8183294	533435	9649170	17.193	44.571	-96.14%	38.83%	43.36%

TABLE II
NON-UNIFORM MESH FLOORPLAN AND P/G CO-SYNTHESIS RESULTS

Circuit	Tiers	Area (um^2)	Deadspace (um^2)	Wirelength (um)	P/G Area (um)	Avg IR Drop (mV)	Max IR Drop (mv)	P/G Area vs 2D	Avg IR Drop vs 2D	Max IR Drop vs 2D
$ami33$	1	2144583	988133	183869	1392195	60.369	132.783	-	-	-
	2	1192783	1229115	139647	1905105	41.665	100.815	-47.55%	30.08%	23.23%
	3	844356	1376617	118414	2641875	36.453	83.637	-104.61%	38.83%	36.31%
	4	636216	1388414	116095	3331950	40.175	99.034	-158.05%	32.58%	24.58%
$apte$	1	59634951	13073323	841105	5978040	32.739	73.588	-	-	-
	2	33837308	21112988	707557	10224750	39.510	96.855	-31.95%	6.25%	15.56%
	3	23820011	24898405	577274	14915670	31.379	87.731	-92.49%	25.54%	23.52%
	4	15508714	15473228	474003	13732140	27.646	81.225	-77.22%	34.40%	29.19%
$xerox$	1	25717209	6366913	1085891	4919565	28.109	78.686	-	-	-
	2	14330332	9310368	699783	6526200	18.794	61.943	-30.02%	34.08%	22.82%
	3	9757603	9922512	610275	8932740	17.401	52.810	-77.96%	38.97%	34.20%
	4	8041782	12816832	524265	10035120	15.010	43.616	-99.92%	47.36%	45.66%

and evaluating 3D IC's effect on 3D P/G networks, a more efficiently designed P/G network can be developed, improving the performance of the entire design.

VII. ACKNOWLEDGEMENT

This work was supported in part by NSF 0903432 and a grant from SRC. Yu Wangs work is partly supported by the National Key Technological Program of China (2008ZX01035-001), NSFC 60870001, and TNList Crossdiscipline Foundation.

REFERENCES

[1] Kerry Bernstein. New dimension in performance. *EDA Forum*, 3(2), 2006.

[2] K. Bernstein, et al. Interconnects in the third dimension: design challenges for 3D ICs. *Proceedings of Design Automation Conference*, pages 562–567, 2007.

[3] W. Rhett Davis, John Wilson, Stephen Mick, Jian Xu, Hao Hua, Christopher Mineo, Ambarish M. Sule, Michael Steer, and Paul D. Franzon. Demystifying 3D ICs: the pros and cons of going vertical. *IEEE Design and Test of Computers*, 22(6):498– 510, 2005.

[4] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat. 3D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. *Proceedings of the IEEE*, 89(5):602–633, 2001.

[5] S. Das, A. Chandrakasan, and R. Reif. Design tools for 3D integrated circuits. *Proceedings of Asia and South Pacific Design Automation Conference*, pages 53–56, 2003.

[6] P. Zhou, Y. Ma, Z. Li, R. P. Dick, L. Shang, H. Zhou, X. Hong, and Q. Zhou. 3d-staf: Scalable temperature and leakage aware floorplanning for three-dimensional integrated circuits. *Proceedings of International Conference on CAD (ICCAD)*, 2007.

[7] Z. Li, X.Hong, Q. Zhou, S. Zeng, J. Bian, H. Yang, V. Pitchumani, and C.K. Cheng. Integrating dynamic thermal via planning with 3D floorplanning algorithm. *Proceedings of Intl. Symp. on Physical Design(ISPD)*, pages 178–185, 2006.

[8] Jason Cong, Ashok Jagannathan, Yuchun Ma, Glenn Reinman, Jie Wei, and Yan Zhang. An automated design flow for 3D microarchitecture evaluation. *Proceedings of Asia and South Pacific Design Automation Conference*, pages 384–389, 2006.

[9] Brent Goplen and Sachin Spatnekar. Placement of 3d ics with thermal and interlayer via considerations. *Design Automation Conference* , pages 626–631, 2007.

[10] Chen-Wei Liu and Yao-Wen Chang. Floorplan and power/ground network co-synthesis for fast design convergence. *Proceedings of international symposium on Physical design*, pages 86–93, New York, NY, USA, 2006. ACM.

[11] W. L. Hung, G. M. Link, Xie Yuan, N. Vijaykrishnan, and M. J. Irwin. Interconnect and thermal-aware floorplanning for 3d microprocessors. *Proceedings of International Symposium on Quality Electronic Design*, page 6 pp., 2006.

[12] J. Cong, Jie Wei, and Yan Zhang. A thermal-driven floorplanning algorithm for 3d ics. *Proceedings of International conference on Computer-aided design*, pages 306–313, 2004.

[13] Jill H.Y. Law, Evangeline F.Y. Young, and Royce L.S. Ching. Block alignment in 3D floorplan using layered TCG. *Proceedings of ACM Great Lakes symposium on VLSI*, pages 376–380, 2006.

[14] J.M. Minz, E. Wong, M. Pathak, and S.K. Lim. Placement and routing for 3D system-on-package designs. *IEEE Transactions on Components and Packaging Technologies*, 29(3):644–657, Sept. 2006.

[15] Eric Wong, J. Minz, and Sung Kyu Lim. Multi-objective module placement for 3-d system-on-package. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 14(5):553–557, May 2006.

[16] E. Wong, J. Minz, and Sung Kyu Lim. Effective thermal via and decoupling capacitor insertion for 3d system-on-package. *Proceedings of Electronic Components and Technology Conference*, pages 1795–1801, June 2006.

[17] Hao Yu, Joanna Ho, and Lei He. Simultaneous power and thermal integrity driven via stapling in 3d ics. *Proceedings of International Conference on CAD (ICCAD)*, pages 802–808, 2006.

[18] Yun-Chih Chang, Yao-Wen Chang, Guang-Ming Wu, and Shu-Wei Wu. B*-trees: a new representation for non-slicing floorplans. *Proceedings of Design Automation Conference*, pages 458–463, 2000.

[19] Laung-Terng Wang, Kwang-Ting (Tim) Cheng, and Yao-Wen Chang. *Electronic Design Automation: Synthesis, Verification, and Test*. Morgan Kaufmann, 2008.

[20] S. Kirkpatrick, C. D. Gelatt, and M. P. Vecchi. Optimization by simulated annealing. *Science*, 220:671–680, 1983.