NBTI-Aware Statistical Circuit Delay Assessment

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Abstract

This work establishes an analytical model framework to account for the NBTI aging effect on statistical circuit delay distribution. In this paper, we explain how circuit NBTI mitigation techniques can account for this extra variability and further present the impact of statistical PMOS NBTI DC-lifetime variability on the product delay spread.

1. Introduction

Negative Bias Temperature Instability (NBTI) is one of the major reliability degradation mechanisms in advanced CMOS technology. Aggressive gate dielectric scaling, lower rate of supply scaling and increasing power density with technology has throttled NBTI induced PMOS threshold voltage shift (ΔV_t) leading to increasing shift in product delay within its lifetime. On top of this, manufacturing variability introduces additional perturbation in device parameter as well as NBTI DC-lifetime of PMOS [1] within and across different dies thus increasing the multiplicity of the problem. There are separate works modeling statistical circuit delay [2] and circuit NBTI aging [3] respectively. In this paper, we combine various sources of variability including NBTI, manufacturing process variation, and PMOS NBTI statistical DC-lifetime variation towards assessing the statistical distribution of circuit delay during its lifetime. With the ever-increasing yield constraints and reliability issues with technology scaling, it makes the combined NBTI and process variation analysis more relevant and important.

NBTI aging has been widely studied at device level focusing on its measurement techniques, physical modeling, and simulation [4,5]. On the other hand, circuit NBTI studies have focused on developing circuit NBTI models [3], augmenting synthesis tools with NBTI awareness [6], building on-chip aging sensors [7,8], and developing custom design technique to increase circuit lifetime [3].

Similarly, study on manufacturing variability focuses on modeling, characterization, and simulation both at device and design level [2,9]. At the design level, the research focuses on statistical CAD algorithms and process variation aware designs [2]. After fabrication the effects due to process variation remains constant. However, when coupled with the time-varying NBTI aging mechanism the statistical device and circuit parameters are bound to change. In addition to this, variability in PMOS NBTI DC-lifetime itself across different PMOS transistors on the same die would add on to the already existing process variability. In this regard the work makes following contributions.

1. An analytical framework to understand the effect of NBTI aging on statistical device parameter and gate delay is developed.
2. The impact of previously proposed circuit NBTI mitigation techniques in statistical domain is analyzed.
3. Finally, the effect of PMOS NBTI DC-lifetime variability on product delay spread with technology scaling is presented.

2. Experimental Setup

The NBTI induced PMOS V_t degradation (positive shift in absolute value of PMOS threshold voltage) is considered to be a combination of slow interface trapped and fast-hole-trapped charges in advanced technology (equation (1)). The slow NBTI induced PMOS V_t degradation is modeled as a power law (equation (2)) in accordance with the reaction diffusion theory, while the fast stress behavior that is attributed to the hole-trapping/de-trapping mechanism saturates at low voltages within few milliseconds [5]. At long stress periods slow interface trapped charges dominates aging hence we neglect fast-hole-trapped charges in our study.

$$\Delta Vt_{stress} = \Delta Vt_{it} + \Delta Vt_h \qquad \text{---(1)}$$

$$\Delta Vt_{it} = \Delta Vt_0 * e^{\left(A * Vgs\right)} * e^{\left(E_a / K_b T\right)} * t^n \qquad \text{---(2)}$$

Where fitting parameters (ΔVt_0, and A), activation energy (Ea), Boltzmann constant (K_b), stress voltage (Vgs), operational temperature (T) and time exponent (n=1/6 in accordance with reaction-diffusion theory) are used in modeling the NBTI behavior due to slow interface trapped charges. One has to incorporate also the recovery model to understand the AC behavior of the NBTI induced V_t stress in PMOS transistors. Universal recovery model is used in our analysis as proposed by Kaczer et al. [10] that follows from equation (3).

$$r(\xi) = 1 / \left(1 + B\xi^{\beta}\right) \qquad \text{---(3)}$$

$$\xi = 1/DF - 1 \qquad \text{---(4)}$$

$$\Delta Vt_{AC} = R * r(\xi) + P \qquad \text{---(5)}$$

Where DF is the duty factor, B is the scaling parameter and β is the dispersion parameter [10]. The total NBTI ΔV_t stress is considered to be a summation of permanent (P, permanent interface traps) and recoverable (R, recoverable interface traps) component (equation (5)), while the r (ξ) describes the duty factor dependence of the recovery as shown in equation (4). NBTI AC/DC factor derived from the above stress/recovery models is fed into the spice simulator for circuit lifetime extraction (Figure 1).

To predict complex digital circuit lifetime we synthesize ISCAS'85 benchmark circuits to the digital libraries and critical paths covering top 10% of the max delay were extracted. We statically calculate the V_t degradation at each transistor using 0.5 static signal probabilities at the circuit primary inputs. The NBTI induced V_t degradation is incorporated by adjusting the DELVTO parameter in HSPICE (using public domain BSIM4 model-card [11]) to obtain aged critical path delay.

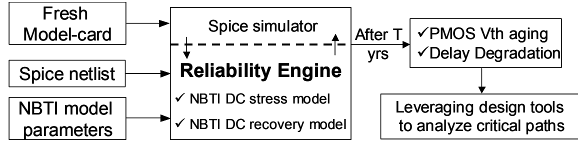

Figure 1: Circuit NBTI simulation setup

Process variation can be subdivided into global and local variation. Global variation encompasses inter-die, inter-wafer, and inter-lot variation, while the local variation covers the within-die (WID) variations. WID variation has random and correlated component. The sources of variation are modeled through Leff, Weff, Tox, and V_t (assuming Gaussian distribution) to precisely analyze statistical circuit characteristics. Monte-Carlo simulation (1000 runs) using HSPICE simulator (with public domain BSIM model-card [11]) was performed to obtain 3-sigma variation on transistor and circuit parameters.

2. Effect of NBTI Aging on Statistical Device Parameters

One can generically assume that the manufactured products to consist of transistors with their parameters (I_{dsat} / V_t) falling within a certain range of spread defined by 3-sigma variation (or 0.1% worst-case/best-case value). However, this statistical spread shifts with device NBTI aging leading to more devices shifting out of the time0 statistical 3σ spread of fresh device parameters (Figure 2).

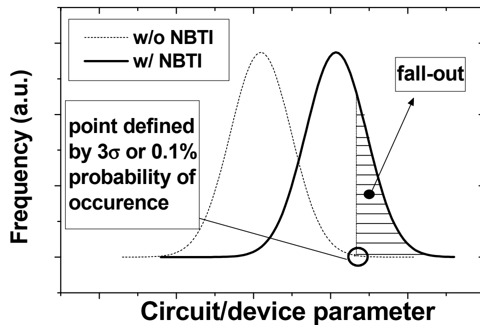

Figure 2: Circuit delay or device parameters (I_{dsat} or V_t) falling-out due to NBTI (Animation)

Thus NBTI induced aging could lead to a shift in the mean, sigma, or both in the device parameters as well as the circuit delay. To capture both the shift in mean and sigma we arbitrarily define a term called fall-out (Figure 2) to gauge the effect of NBTI on statistical PMOS device parameter (I_{dsat}) and also the circuit parameter (delay). The fall-out is another way of looking at the device or circuit aging due to NBTI in a statistical domain and hence should not be confused with a failure indicator.

Figure 3 briefly illustrates the effect of NBTI aging on the statistical I_{dsat} and V_t spread of PMOS device of different gate widths. We call the PMOS devices with their I_{dsat} moving out of the 3σ spread of fresh PMOS statistical I_{dsat} distribution as a result of NBTI as I_{dsat} fall-outs. At the device level, I_{dsat} is chosen as fall-out indicator, as it is one of the major decider of transistor delay.

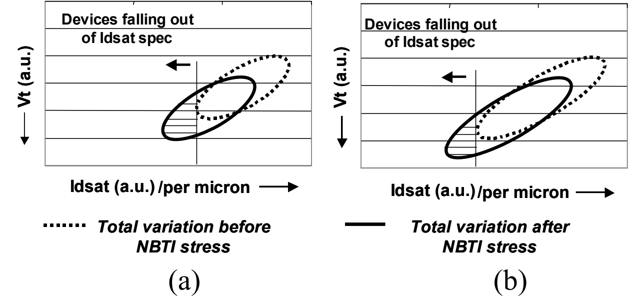

Figure 3: (Illustration) I_{dsat} versus V_t distribution of fresh devices shifting due to NBTI aging in larger width PMOS (a) and smaller width PMOS (b).

Figure 3a and 3b shows that the percentage I_{dsat} fall-out for a larger width PMOS device is higher compared to smaller width PMOS. The reason being that, local variation (mismatch) is inversely proportional to the square root of effective gate length and width of the transistor [9]. This implies that, larger width PMOS has lesser I_{dsat} variation. Though NBTI induced I_{dsat} shift is independent of transistor width, the I_{dsat} shift relative to the I_{dsat} variation differs with transistor widths and hence the difference in I_{dsat} fall-outs between larger and smaller width PMOS (figure 3).

Secondly, we analyze the effect of aging on I_{dsat} fall-outs with time. NBTI aging with time is represented in terms of ΔV_t, which is widely used to track the effect of NBTI induced core PMOS device [5] parameter variations. While the device fall-outs due to NBTI were calculated using the I_{dsat} parameter (for short-channel) that is used as an indicator for device performance.

$$I_{dsat} = Cox * \upsilon * (Vgs - V_t - \Delta V_t) \quad \text{---(6)}$$

$$f(V_t) = \frac{1}{\sigma\sqrt{2\pi}} e^{\left[\frac{-(V_t - \mu_{v_t})^2}{2\sigma_{v_t}^{\,2}}\right]} \quad \text{---(7)}$$

Assuming a Gaussian distribution for V_t (equation (7)), one can derive the Probability Density Function (PDF) of I_{dsat} (equation (8)) based on I_{dsat} equation (6). Assigning, $A = Cox * \upsilon * Vgs$, and $B = Cox * \upsilon$, where Cox is gate capacitance and ν is saturation velocity, we get,

$$f(I_{dsat}) = \frac{1}{B\sigma\sqrt{2\pi}} e^{\left[-\left(\frac{I_{dsat}-A}{B} - (\mu_{v_t} + \Delta V_t)\right)^2 \Big/ 2\sigma_{v_t}^{\,2}\right]} \quad \text{---(8)}$$

$$F(I_{dsat}) = 0.5*\left(1+erf\left(\frac{\frac{I_{dsat}-A}{B}-\left(\mu_{V_t}+\Delta V_t\right)}{\sigma_{V_t}*\sqrt{2}}\right)\right) \quad \text{---(9)}$$

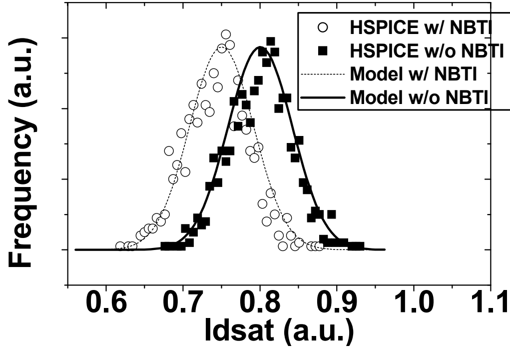

Figure 4: I_{dsat} PDF distribution (model and HSPICE based Monte-Carlo simulation) before and after NBTI induced ΔV_t shift on PMOS.

Figure 4 shows close match between the analytical model for PDF of I_{dsat} ($f(I_{dsat})$) and HSPICE. The I_{dsat} fall-out is calculated as the area under NBTI shifted $f(I_{dsat})$ that falls outside of $f(I_{dsat})$ of a fresh PMOS device calculated using the Cumulative Distribution Function (CDF) from equation (9). Basically the I_{dsat} fall-outs follow a trend characteristic of an error function (erf) (Figure 5).

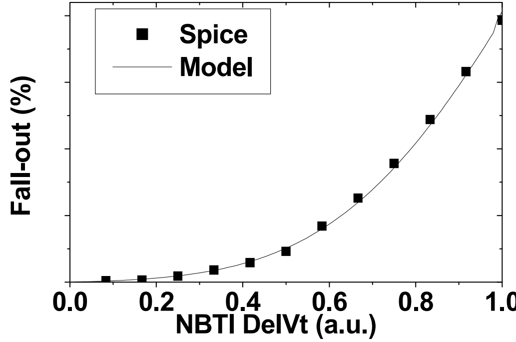

Figure 5: I_{dsat} fallout of PMOS devices with NBTI aging

2. Effect of NBTI Aging On Single/Multi Stage Statistical Gate Delay

PMOS width and NBTI induced ΔV_t has substantial effect on the I_{dsat} fall-outs due to NBTI at the transistor level. At the circuit level NAND, NOR, and INV can be considered as basic building blocks. PMOS NBTI aging differs in the way it affects the delay aging of these three basic gates. It is well known that NBTI aging impacts NOR gate more than the NAND, and INV gate delay. The reason being that the PMOS stacking in NOR is more vulnerable to delay aging due to stacking effect [3].

In this regard, the rise-delay fall-out of basic gates is analyzed applying global and local variation (we assume that all the PMOS in the gate are fully correlated and the same for NMOS) to the individual gates. Linear approximation model for gate delay (T_d shown in equation (10)) is used in both circuit NBTI aging models [6] as well as statistical circuit delay models [2].

$$T_d = B*V_t + C \quad \text{---(10)}$$

B, and C are constants associated with the process parameters, load and biasing conditions of the devices. However when analyzing the NBTI effect on statistical delay spread we found that the linear gate delay model under-predicts the gate-delay fall-outs. We derive our delay fall-out model based on the gate delay model (following a alpha-power law based CMOS inverter delay model [12], where alpha is assumed to be equal to 1) shown in equation (11) to explain this.

$$Td = \frac{A}{(V_{gs}-V_t-\Delta V_t)} \quad \text{---(11)}$$

Where, $$A = \frac{C_{total}*V_{dd}}{n*\upsilon*C_{ox}} \quad \text{---(12)}$$

Where C_{total} is output load capacitance and n is a fitting parameter. Assuming that the V_t distribution follows Gaussian (equation (13)), one can derive the PDF of T_d to analyze the effect of NBTI induced V_t increase on the T_d distribution and the ensuing rise-delay fallouts.

$$f(V_t) = \frac{1}{\sigma\sqrt{2\pi}} e^{\left[\frac{-(V_t-\mu_{v_t})^2}{2\sigma_{v_t}^2}\right]} \quad \text{---(13)}$$

$$f(T_d) = \frac{A}{T_d^2} * \frac{e^{\left[\frac{-\left(Vgs-\frac{A}{Td}-\left(\mu_{v_t}+\Delta V_t\right)\right)^2}{2\sigma_{v_t}^2}\right]}}{\sigma_{V_t}\sqrt{2\pi}} \quad \text{---(14)}$$

$$F(T_d) = 0.5*\left(1+erf\left(\frac{Vgs-A/T_d-\left(\mu_{V_t}+\Delta V_t\right)}{\sigma_{V_t}*\sqrt{2}}\right)\right) \quad \text{---(15)}$$

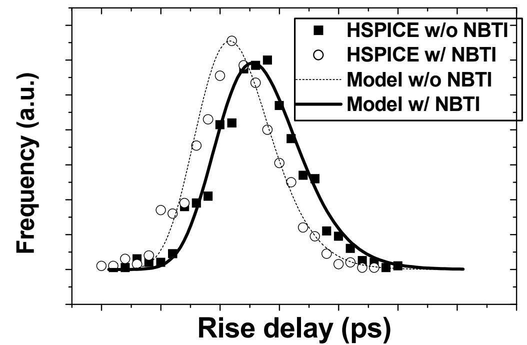

Figure 6: INV rise delay (T_d) PDF distribution (model and HSPICE based Monte-Carlo simulation) before and after NBTI

We can draw two observations about the PDF distribution of Inverter rise-delay (T_d) from Figure 6. First one being that the PDF of T_d distribution (equation (14)) is non-Gaussian with a long tail. Secondly, NBTI induced V_t increase not only

shifts the mean of $f(T_d)$ but also increases its spread (or sigma) (Figure 6). However assuming a linear V_t dependent transistor delay model (equation (10)), would have underestimated the delay fall-out. That is, with a linear delay model, an input Gaussian $f(V_t)$ would have lead to a Gaussian $f(T_d)$. In which case a NBTI induced ΔV_t shift ($\mu_{Vt}+ \Delta V_t$) would only have lead to a shift in mean value of T_d, but not an increase in its spread (sigma) thus underestimating the delay fall-outs.

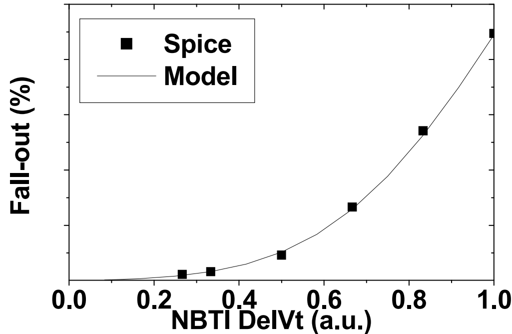

Figure 7: Inverter rise delay fall-out (model and HSPICE based prediction) due to NBTI aging of INV

With NBTI induced ΔV_t shift (while keeping σ_{Vt}, A, and Vgs as constants), the inverter rise-delay fall-out increase following a trend that is characteristic of an error function (*erf*) (Figure 7). Note that the rise-delay fall-out here indicates the area under NBTI shifted $f(T_d)$ that falls outside of $f(T_d)$ of inverter with fresh device calculated using the CDF from equation (15). One can extend the statistical inverter rise-delay fall-out model to take care of NOR and NAND gates by adjusting V_t, A, and B to match with the HSPICE Monte-Carlo prediction.

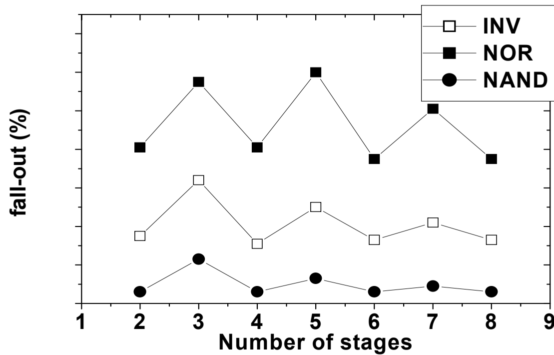

Figure 8: INV/NOR/NAND chain rise-delay fall-out (HSPICE based Monte-Carlo simulation) at the end of 10yrs due to NBTI induced PMOS ΔV_t aging

Figure 8 shows the INV/NAND/NOR chain circuit rise-delay fall-outs with increasing number of stages. The rise-delay here means the primary output rising delay. The rise-delay fall-out simulations were carried with an input static signal probability of 0.5. Three main observations can be drawn from the simulated HSPICE predictions in Figure 8. Firstly, the NAND/INV/NOR has increasing delay fall-outs in the order mentioned, due to the decreasing strength of pull-up (PMOS) network relative to the pull-down network leading to increasing NBTI vulnerability. Secondly, the odd stages have higher delay fall-outs due to the presence of an excess pull-up node in the rise-delay path in comparison to the pull-down nodes leading to more (%) delay aging and hence fall-outs. Thirdly, the rise-delay fall-outs of larger stage chains converge to the fall-out value of 2-stage chains as the ratio of pull-up to pull-down nodes in larger chain approaches one.

A complete analytical model to predict the delay fall-outs for multi-stage circuit would save time on the cumbersome HSPICE based Monte-Carlo runs. Model prediction for multi-stage circuit delay fall-outs is currently under progress and will be available in the future works. In our next section, we use HSPICE based Monte-Carlo predictions to study the effect of NBTI on statistical delay of complex digital circuits that contains multiple stages. And based on our single stage circuit delay fall-out prediction model, the HSPICE prediction trends are analyzed.

2. Effect of NBTI Aging On Statistical Circuit Delay

We synthesize complex logic circuits (ISCAS'85 benchmarks) using basic NBTI characterized libraries (INV/NAND/NOR) of varying transistor widths, stacks and fingers. Spice netlist of the circuits were augmented with Leff, Weff, Tox, and V_t variations that incorporate global (variation across die) and local (random, and correlated component within die) variations. The above-mentioned spice parameters that were used to model the total variation are assigned mean and standard deviations (following a Gaussian distribution) such that larger width transistors would observe a 10% I_{dsat} shift from the mean at the 3-sigma point. Further the local variation (mismatch) dependence on Leff, and Weff is modeled based on the empirical expression proposed by Asenov et al [9]. In our simulation either we allow the circuits to have total random local variation or total correlated local variation (meaning there is no WID spatial variation) to understand the difference between the NBTI interaction with the two extremes though in reality there will be a mix of both.

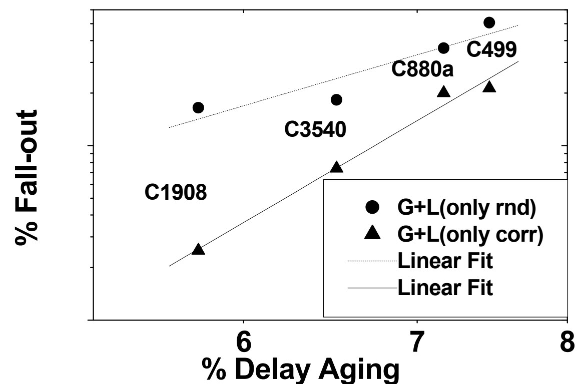

Figure 9: ISCAS'85 benchmark critical path delay aging and fall-out at the end of 10yrs (HSPICE based Monte-Carlo prediction) due to NBTI (Note: G (L) denotes global (local) variation)

HSPICE based Monte-Carlo simulation was performed on time (0) and time (10yrs) NBTI aged circuits with a PMOS NBTI induced ΔV_t =45mv @ 10yrs for a PMOS in a circuit with 50% input duty cycle. Two main observations can be drawn from the NBTI induced delay fall-out prediction at the end of 10yrs for the ISCAS'85 benchmarks shown in Figure 9. Namely, the power-law dependence of circuit delay fall-outs on NBTI induced delay aging and delay standard deviation of its critical path. The behavior of circuit delay fall-outs to NBTI induced delay shift can be understood from a simple inverter rise-delay fall-out behavior without loss of generality.

The Inverter delay fall-out response to PMOS NBTI V_t shift (Figure 7) is re-plotted in Figure 10 in log-log scale, showing the linear fitting closely matching the HSPICE prediction. This linear fitting is attributed to behavior of the error function (*erf*) (within the range of ΔV_t shown in Figure 10) that is used in the calculation of fall-outs for gate delays (equation (15)). In other words, delay fall-out has a power law dependence on NBTI induced PMOS ΔV_t. Additionally, based on a first order linear transistor delay (T_d) approximation model (equation (10)) (note than the statistical mean value of T_d can be approximated with a linear dependence model for the range of ΔV_t shift due to NBTI leading to 10% T_d shift), one can derive a linear relation between the gate delay response and NBTI induced PMOS ΔV_t. Hence delay fall-out is an power-law function of the % delay aging.

This finding has an important bearing on the NBTI mitigation techniques at the circuit level. By making linear changes to the mean delay aging of circuits, one can control the delay fall-outs following the predicted power-law trend in Figure 9. Thus predicting the effectiveness of circuit NBTI mitigation techniques (transistor gate sizing, body biasing, and supply voltage scaling) for circuit delay fall-out improvement with minimal penalty on optimizing only the critical nodes along the critical path of the circuit [6].

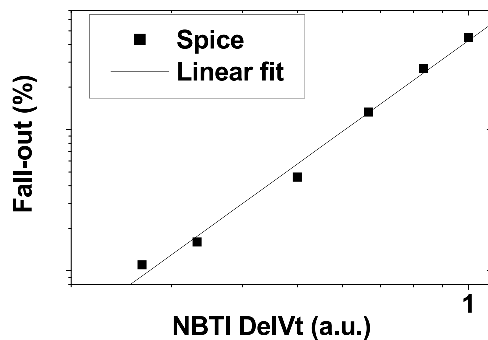

Figure 10: Inverter rise delay fall-out (HSPICE based prediction) due to NBTI aging of INV (Note: Figure 7 re-drawn in log-log scale)

Secondly, NBTI induced delay fall-outs are larger for circuits with local variation component that is completely correlated (correlation factor=1) among all the critical path libraries compared to the completely random local variation counterpart (Figure 9). This can be explained based on the understanding that a completely correlated local variation leads to higher variation in statistical circuit delay compared to the completely random local variation case [13].

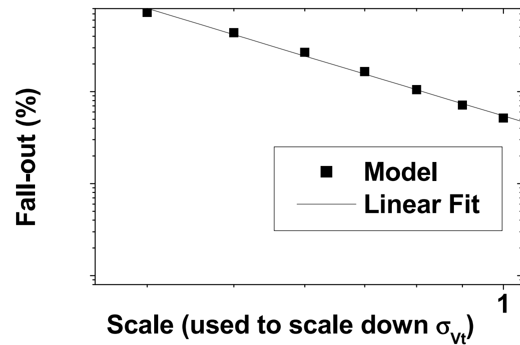

Figure 11: Inverter rise delay fall-out (model from equation (15)) at the end of 10yrs due to NBTI aging (Note: scale value is used to scale down the time0 sigma of PMOS V_t distribution (σ_{Vt}) used in equation (15))

Further, Figure 11 shows a power-law dependence of circuit delay fall-out on the circuit delay spread (sigma) based on the single-stage INV rise delay fall-out model (Equation 15). Hence the difference between the ISCAS'85 delays fall-outs with completely correlated and random local variation case. An important implication of this understanding is that tightening or reduction of statistical circuit delay variation leads to more NBTI induced delay fall-outs and hence the necessity to include more circuit delay guard band.

Finally, we look at circuit delay fall-out sensitivity to NBTI lifetime. Here we define the PMOS NBTI DC lifetime to be the time taken in years of a PMOS device ΔV_t to shift by 50mV under DC stress conditions (using equation (2)) as shown in equation (16). We empirically derive fitting parameter ΔVt_0 from equation (16) for a given PMOS DC lifetime under a given stress voltage (Vgs) and temperature (T) conditions and use it in equation (2) to obtain NBTI PMOS transistor degradation at different times.

$$DC_lifetime = \sqrt[n]{\frac{50mV}{\Delta Vt_0 * e^{(A*Vgs)} * e^{\left(E_a/K_bT\right)}}} \quad \text{---(16)}$$

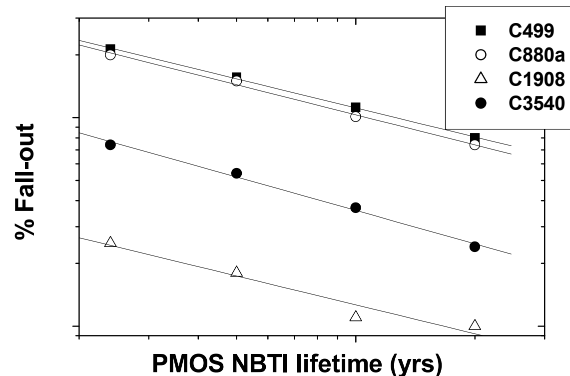

Figure 12: ISCAS'85 benchmark critical path delay fall-out at the end of 10yrs (HSPICE based Monte-Carlo prediction) with varying PMOS NBTI DC lifetimes

NBTI lifetime follows a random distribution in a circuit that can be closely modeled by lognormal statistics [14]. Such a Lognormal NBTI statistics across a circuit can lead to an exponential variation in NBTI lifetime of the libraries in the critical path. To make the understanding simple, we consider the PMOS NBTI DC lifetime of all the PMOS (without incorporating lognormal lifetime distribution) in the circuit to be equal and perform HSPICE based Monte-Carlo simulations (with only-correlated local variation among critical path circuits) to predict the NBTI induced circuit delay fall-outs with NBTI lifetime change. From Figure 12, one can observe that circuit delay fall-outs follow a power-law trend with PMOS NBTI DC lifetime.

This can be explained from Figure 13 (plot derived based on equation (16) and (2)) that shows a power-law dependence of NBTI induced ΔV_t on PMOS NBTI DC lifetime of PMOS device. Additionally, we know from Figure 10 that NBTI induced PMOS ΔV_t and the induced delay fall-outs have power-law relation. Hence transitively, we have the ISCAS'85 delay fall-outs having a power-law dependence on MOS NBTI DC lifetime

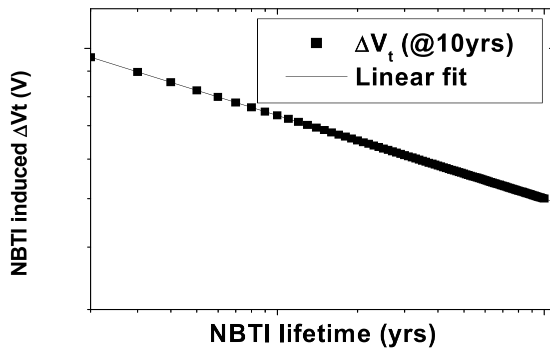

Figure 13: PMOS NBTI DC lifetime (lifetime=time @ PMOS NBTI induced ΔV_t=50mv) versus the corresponding NBTI induced PMOS ΔV_t @ 10yrs

Thus exponential variation of PMOS NBTI DC lifetime in critical path libraries leads to exponential variation of NBTI induced delay fall-outs. Further with technology scaling, PMOS NBTI DC lifetime variability gets critical [1] and hence the necessity to model NBTI lifetime variability into the statistical circuit delay fall-out prediction framework. Such a complete model framework will help attack NBTI reliability concerns at the design level in presence of process and NBTI lifetime variability.

2. Conclusion

In this paper, we established a framework to link the effect of NBTI aging and statistical PMOS transistor parameter (I_{dsat}) shift, to delay distribution of library cells and more complex circuits. Circuit delay fall-out (-of time0 manufacturing 3σ statistical spread of product delay) is predicted to have power-law dependence on the NBTI induced PMOS ΔV_t shift. Circuit NBTI mitigation techniques (transistor gate sizing, body biasing, and supply voltage scaling) are expected to account for this effect with minimal cost penalty by optimizing only the NBTI vulnerable nodes. Additionally, the presence of PMOS NBTI DC random lifetime variability is predicted to increase the circuit delay fall-outs following a power-law dependence, which becomes critical with technology scaling.

9. References

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