



Variation-Aware Supply Voltage Assignment for Minimizing Circuit Degradation and Leakage

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Outline

- **Background: Leakage and NBTI**
- Statistical Analysis Flow
- Variation-Aware Supply Voltage Assignment Technique
- Simulation Results
- Conclusion



Background: Leakage

- The circuit total power (P_{total}) can be calculated as:

$$P_{total} = \underbrace{P_{switch} + P_{shortcircuit}}_{dynamic\ power} + \underbrace{P_{leakage}}_{static\ power}$$

- As technology scales, the dynamic power of one transistor decreases, while leakage power increases.
- Leakage is more than 50% of the total power. The modeling and optimization has been studied for 10 years or more.



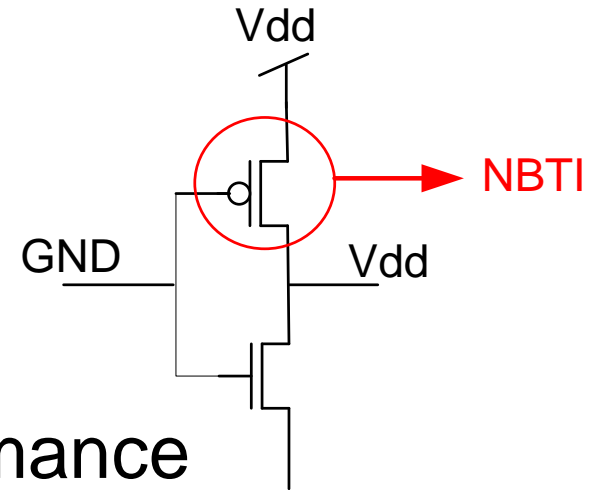
Leakage reduction techniques

- Standby time techniques
 - Power Gating
 - Input Vector Control
 - Body biasing → adapt V_{th} during the standby time
 - Adapt V_{dd} during the standby time
- Run time techniques
 - DVTS dynamic V_{th} scaling
 - DVS dynamic V_{dd} scaling
- Design time techniques
 - Dual V_{th}
 - Dual V_{dd}
 - Gate sizing



Background: Aging due to NBTI

- Negative Bias Temperature Instability
- Conditions
 - PMOS transistor
 - Negatively biased
 - elevated temperature
- Impact of NBTI on circuit performance
 - a shift in threshold voltage
 - a significant increase in the delay of PMOS devices, and result in about 10-20% degradation in circuit speed





NBTI mitigation techniques

- Dynamic Adjustment (V_{dd} , V_{th}) [ASPDAC09]
- NBTI-aware Sizing [DATE06]
- Guard banding [ASPDAC08]
- Lower temperature, V_{dd} , and signal probability [DAC06]
- NBTI-aware Synthesis [DAC07]
- Input Vector control [DATE 07, MICRO 07]
- Internal node control [DATE 2009 *2]
- Memory NBTI mitigation [ISQED06]

*Compensation
Techniques*

*Mitigation
Techniques*



NBTI vs Leakage

- Higher Vdd
- ☹ • Higher NBTI degradation rate
- ☹ • Higher Leakage

Problem: How to assign Vdd so that the **performance** constraint is always satisfied considering **NBTI** and **process variations**, while maintaining a very low **leakage** power consumption

- ☺ • Lower Leakage
- ☹ • Lower Performance

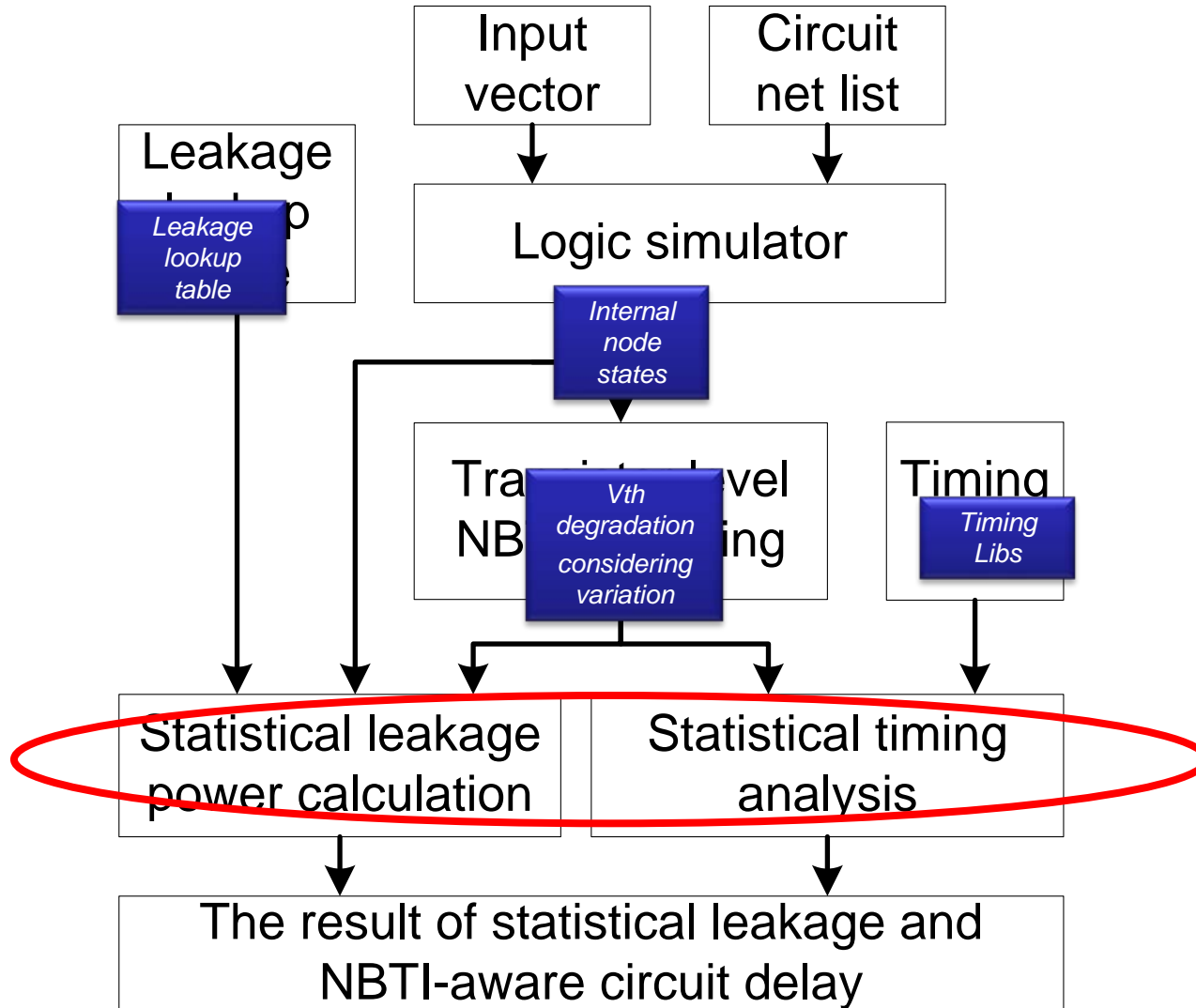


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Statistical Analysis Flow





Statistical Model

- Vth variation model, assume that Vth can be modeled as a Gaussian distribution.

$$PDF(V_{th}) = \frac{1}{\sqrt{2\pi}\sigma_{th}} e^{-\frac{1}{2}\left(\frac{V_{th}-\mu_{th}}{\sigma_{th}}\right)^2}$$

- The threshold voltage of each gate v_i is expressed as linear combinations of its mean value and random variables:

$$V_{i,th} = V_i + a_0\Delta V_i + \sum_{j=1}^n a_j\Delta V_{i+j} + \sum_{j=1}^n a_j\Delta V_{i-j}$$



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Supply Voltage Assignment Technique

- Dual Vdd Assignment and Dynamic Vdd Scaling
- Why dual Vdd?
 - High Vdd is used to compensate for NBTI-induced degradation on critical gates, while low Vdd is used to reduce leakage power on other gates.
- Why dynamic scaling?
 - “One-time” solutions at design time will lead to large power and area overhead.
 - Variations will affect the circuit performance.





Supply Voltage Assignment Technique

- **First Step: Dual Vdd Assignment**

- Two Sets:

- High Vdd Set (HVS)
- Low Vdd Set (LVS)



- HVS includes all the critical paths and their predecessors in order to avoid level converter
- LC penalty can be carefully considered to have more gates in the LVS.



Supply Voltage Assignment Technique

- **Second Step: Dynamic Vdd Scaling**

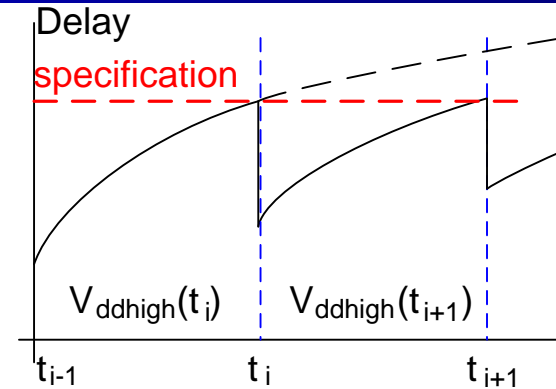
- Determine the **optimal high Vdd**, to ensure NBTI-induced degradation and leakage power are simultaneously minimized during the following time interval

$$F = A \times (\mu_{D(t_{i+1})} + 3\sigma_{D(t_{i+1})}) + B \times (\mu_{L(t_i)} + 3\sigma_{L(t_i)})$$

- Determine the **optimal low Vdd**, to reduce leakage power as more as possible during the following time interval.

$$D_{relax}(v) = D_{current}(v) + C \times D_{slack}(v)$$

- Predict the **next time node** at which the circuit delay will exceed the specification and the supply voltages need to be scaled again. [CICC 2008][ASPDAC2009]



(Assume $t_{i+1} \rightarrow$
 $V_{ddhigh} \rightarrow$ new t_{i+1}
 \rightarrow new $V_{ddhigh} \rightarrow$
... final V_{ddhigh}, t_{i+1})

$$\mu_{Td}(t) = \mu_{Td}(0)(1 + Ct^n)$$



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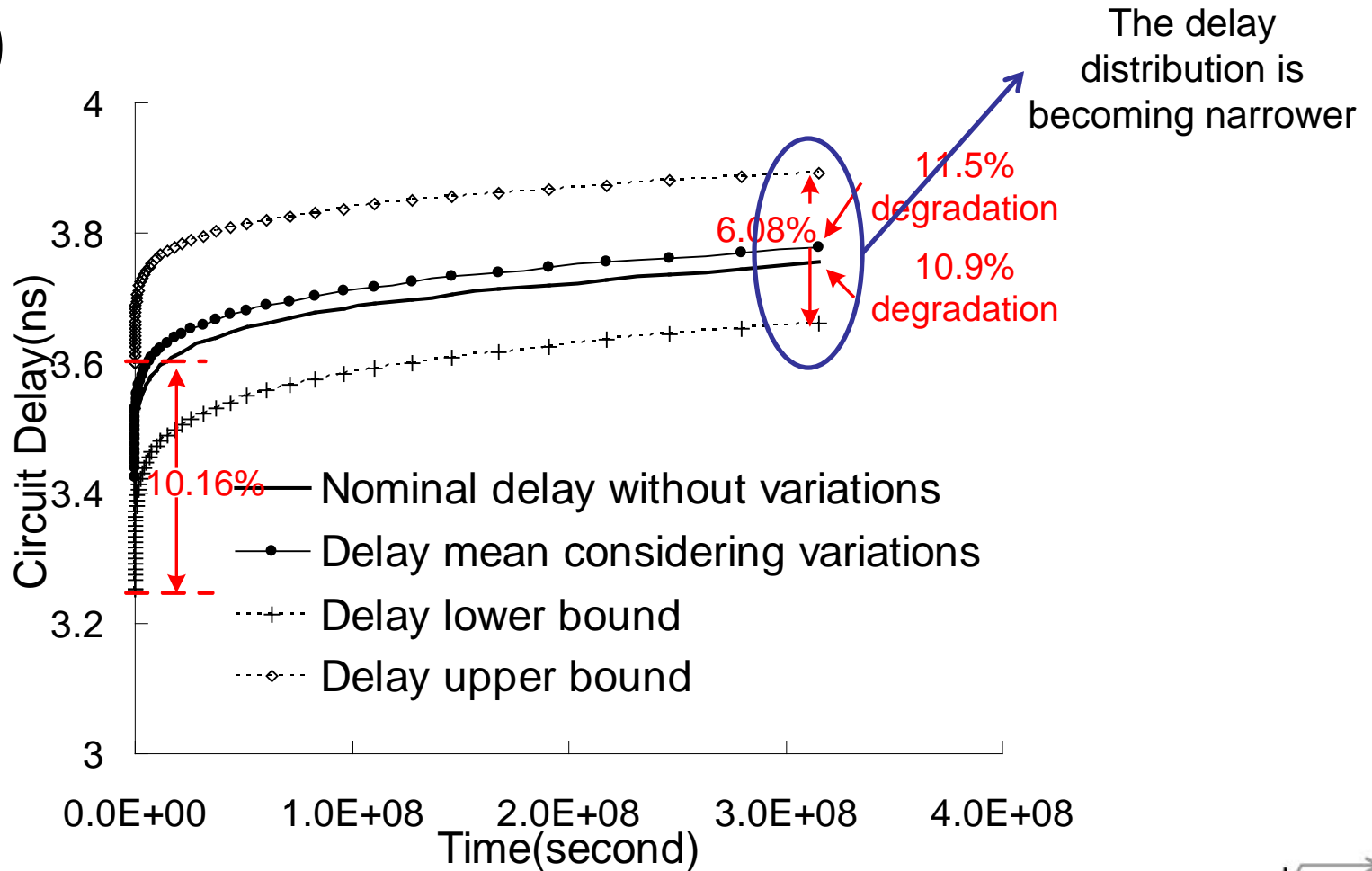
Implementations

- C++ for most of the codes with PrimeTime
- 65nm library
- Some key technology parameters are:
 - Nominal Vdd = 1.0V ; $|V_{th}| = 0.20V$; $T_{ox} = 1.2nm$
- ISCAS85 benchmark and some ALU circuits are used to evaluate our algorithms.
- Temperature is 378K.
- The nominal circuit lifetime is set to be 10 years..



Simulation Results-platform(1)

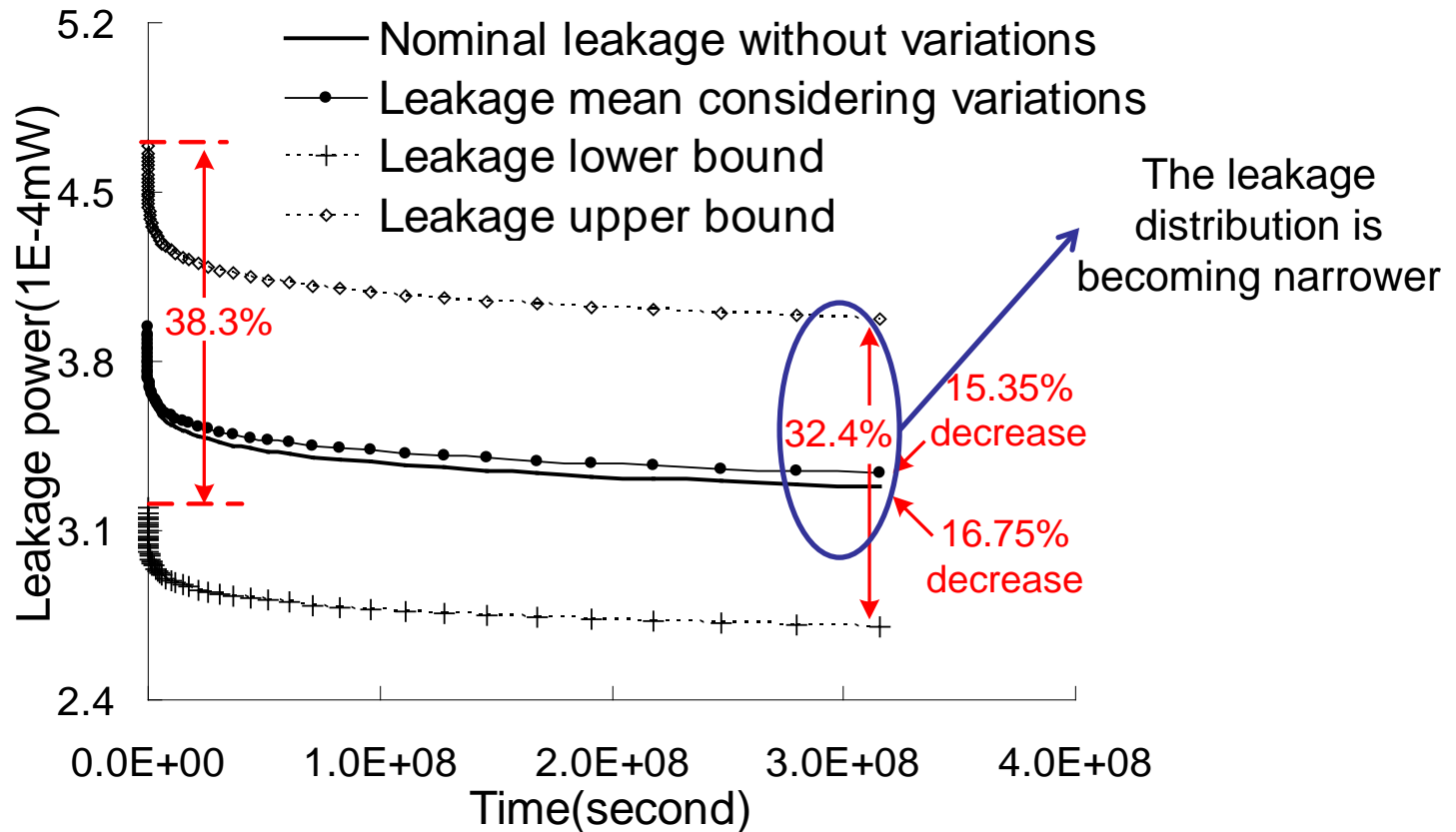
- The impact of variations on NBTI for c880





Simulation Results-platform(2)

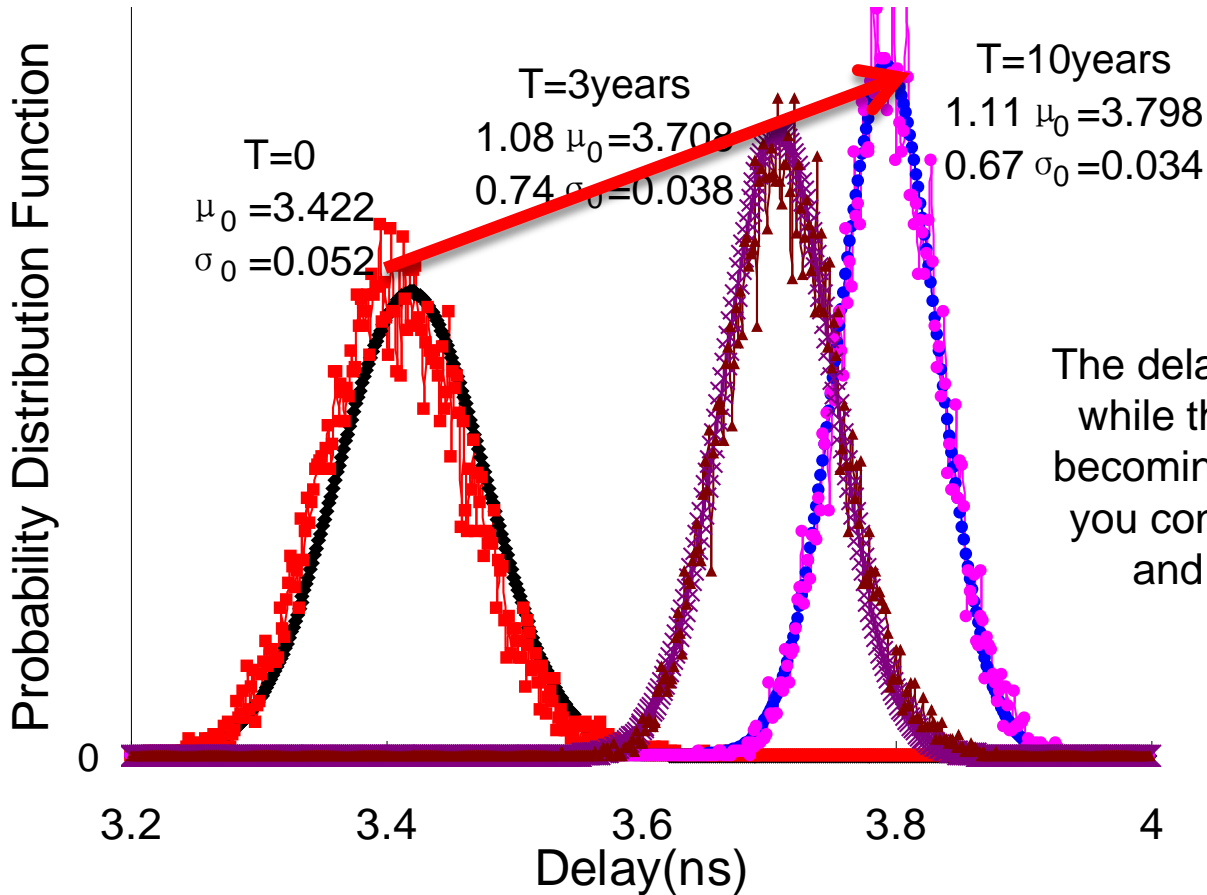
- The impact of variations on leakage power for c880





Simulation Results-platform(3)

- Delay distribution compared to Monte Carlo for c880

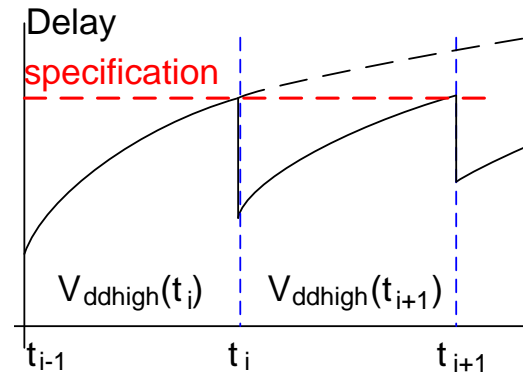
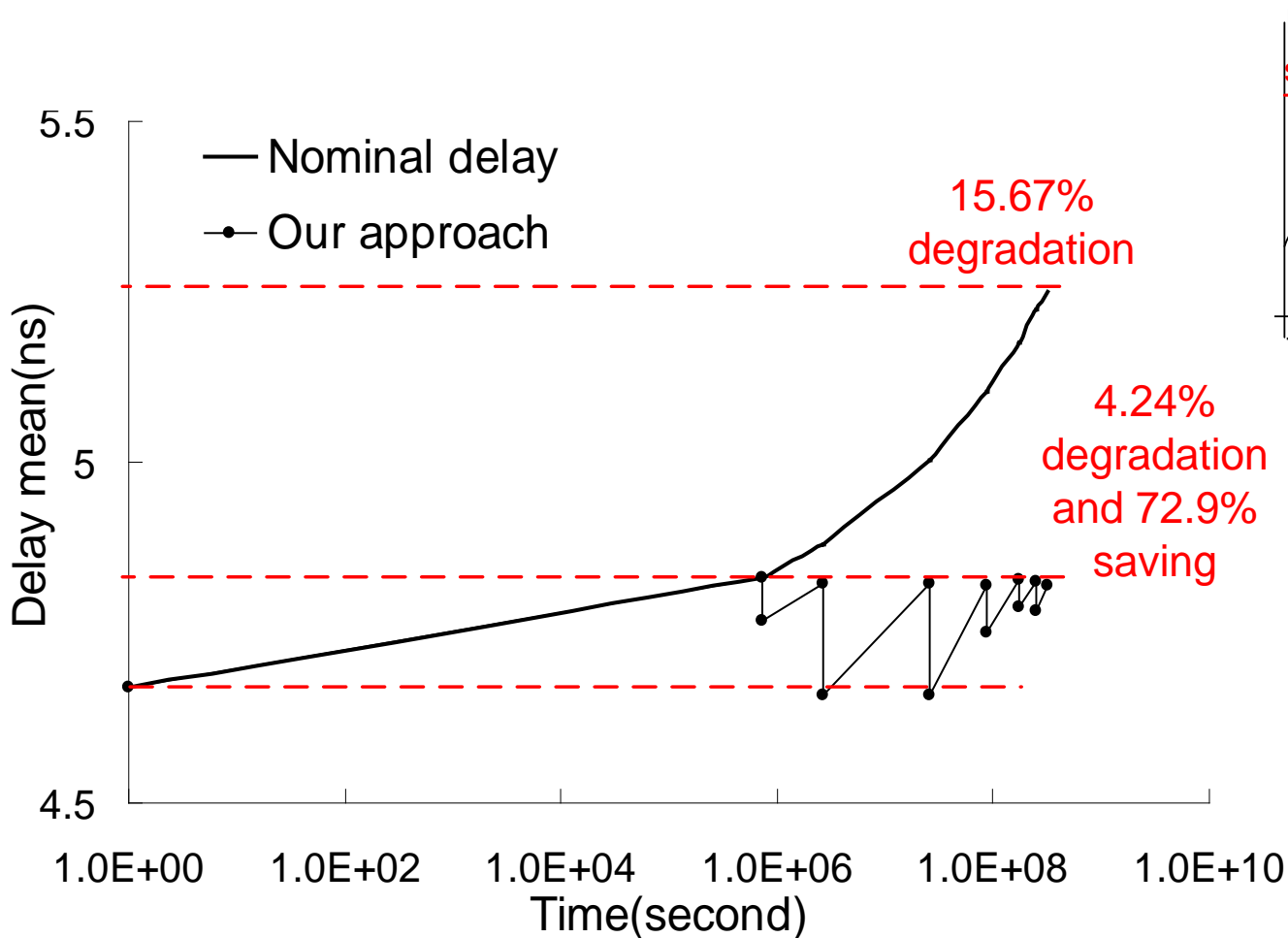


The delay mean is larger, while the distribution is becoming narrower when you consider both NBTI and V_{th} variation



Simulation Results-SVA(1)

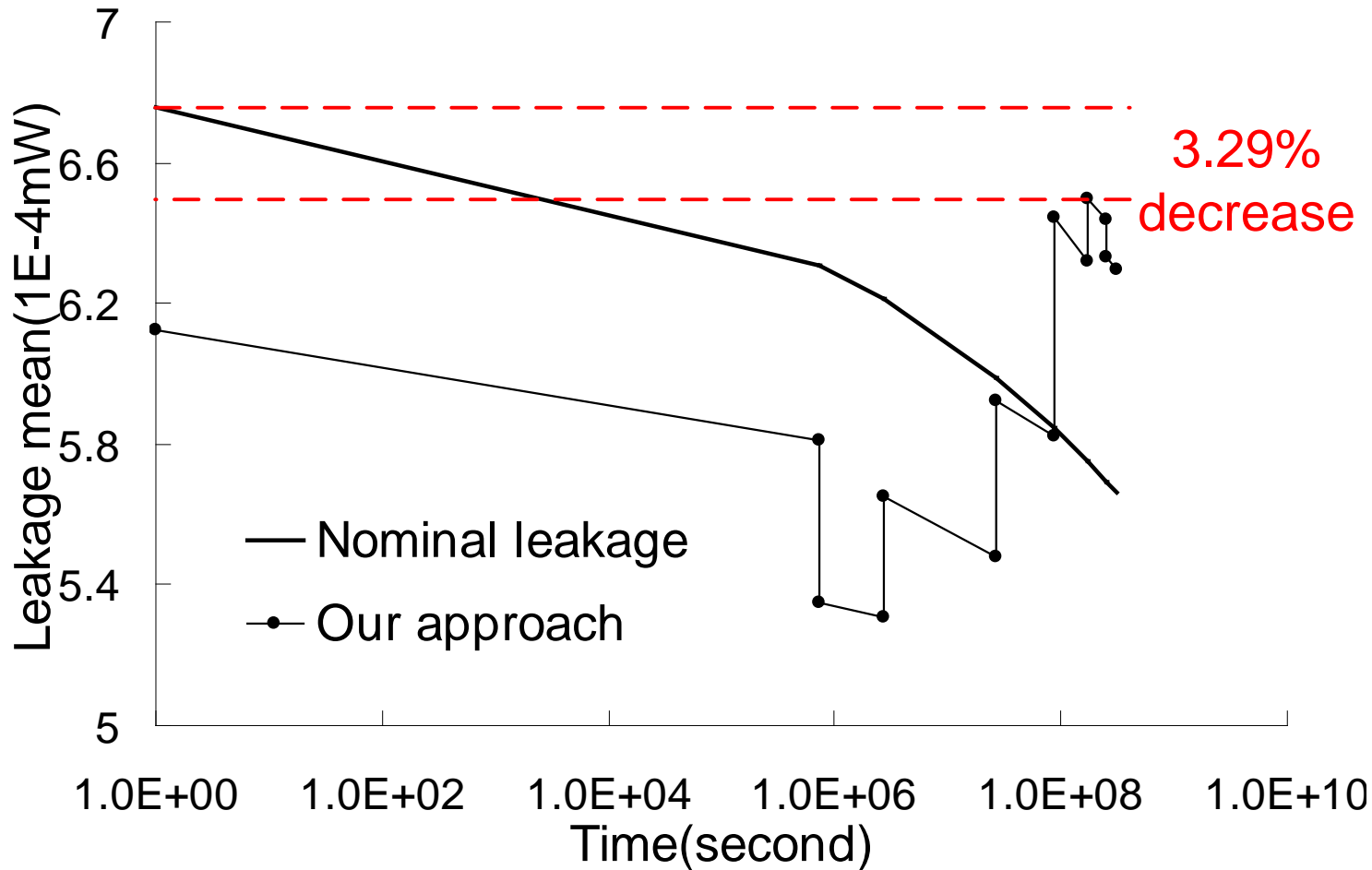
NBTI induced degradation comparison (C1908)





Simulation Results-SVA(2)

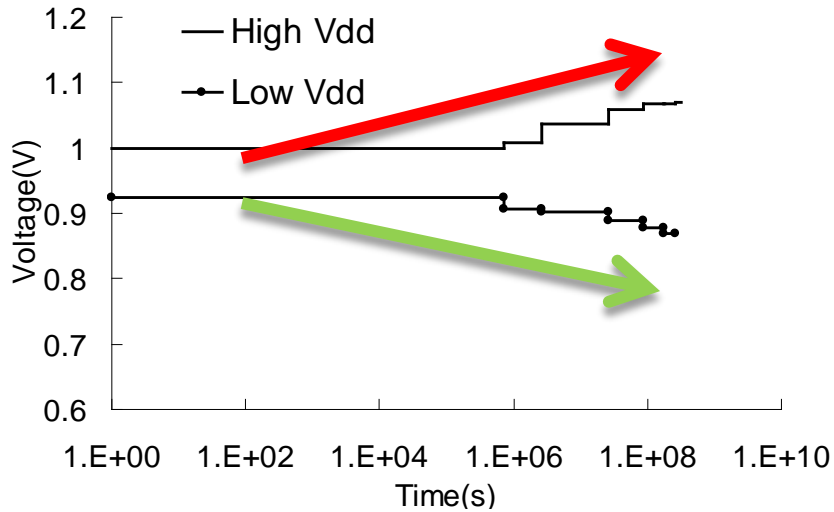
- Leakage power comparison (c1908)



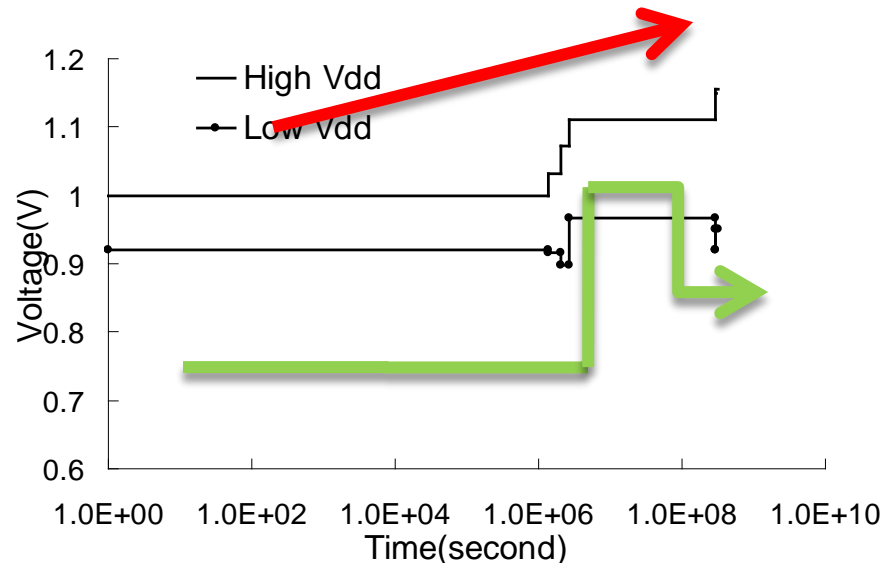


Simulation Results-SVA(3)

- The voltage scaling (c1908 vs c7552)



c1908



c7552



Simulation Results-SVA(4)

Our SVA [⊕]				Single V_{dd} scaling [⊕]				
$D_{imp}(\%)$ [⊕]	L_{max} [⊕]	$L_{inc}(\%)$ [⊕]	$Lv\#$ [⊕]	D_{life} [⊕]	$D_{imp}(\%)$ [⊕]	L_{max} [⊕]	$L_{inc}(\%)$ [⊕]	$Lv\#$ [⊕]
55.63 [⊕]	↔	-4.12 [⊕]	9 [⊕]	↔	60.84 [⊕]	↔	52.38 [⊕]	6.86 [⊕]
52.98 [⊕]	↔	-2.5 [⊕]	9.63 [⊕]	↔	58.98 [⊕]	↔	29.96 [⊕]	7.77 [⊕]

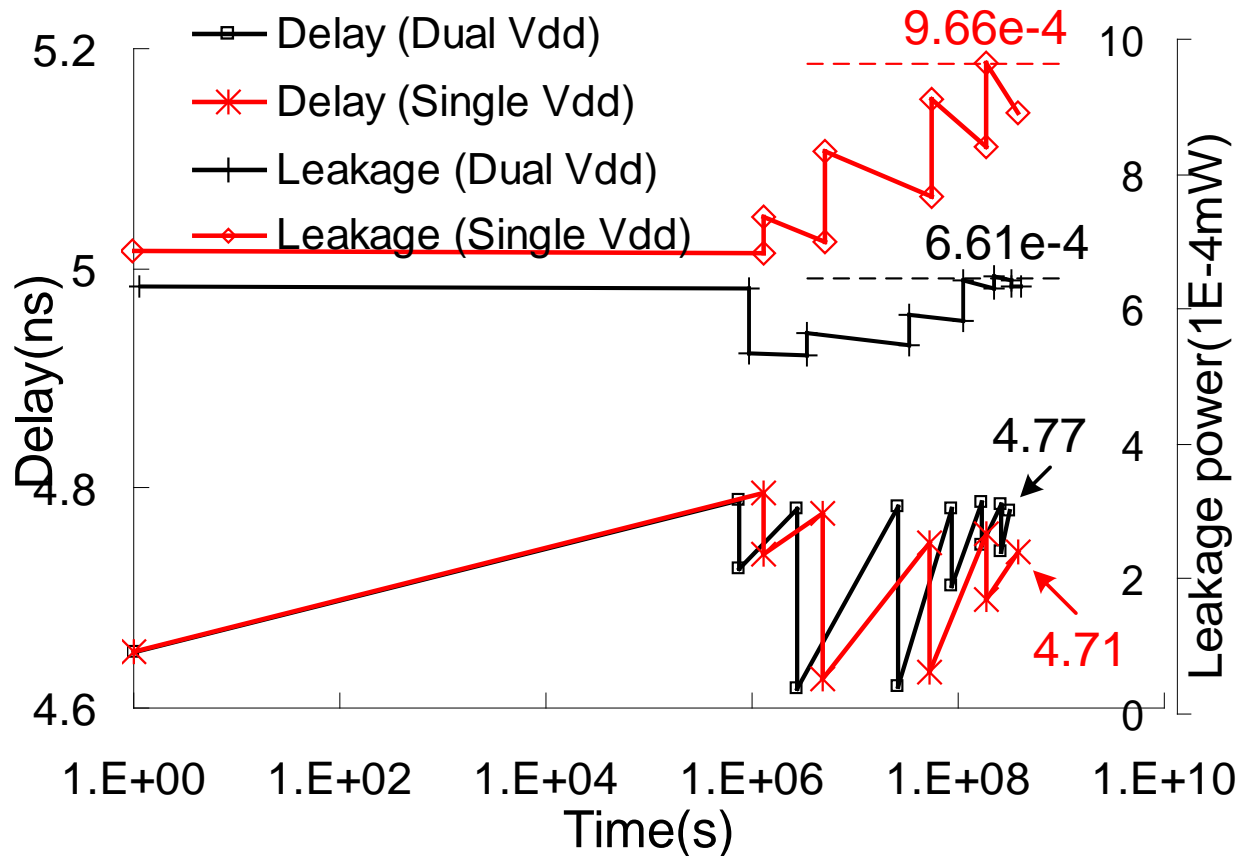
Table 2. The results of our SVA and compare with single V_{dd} scaling[⊕]

circuit [⊕]	Gate# [⊕]	BVSH [⊕]	LVSH [⊕]	D_p [⊕]	Nominal design [⊕]		Our SVA [⊕]					Single V_{dd} scaling [⊕]				
					D_{we} [⊕]	L_p [⊕]	D_{we} [⊕]	$D_{imp}(\%)$ [⊕]	L_{max} [⊕]	$L_{inc}(\%)$ [⊕]	$Lv\#$ [⊕]	D_{we} [⊕]	$D_{imp}(\%)$ [⊕]	L_{max} [⊕]	$L_{inc}(\%)$ [⊕]	$Lv\#$ [⊕]
array4x4 [⊕]	89 [⊕]	76 [⊕]	13 [⊕]	2.485 [⊕]	2.737 [⊕]	9.12E-05 [⊕]	2.597 [⊕]	55.51 [⊕]	8.21E-05 [⊕]	-9.96 [⊕]	7 [⊕]	2.589 [⊕]	58.78 [⊕]	1.00E-04 [⊕]	10.03 [⊕]	6 [⊕]
pmult4x4 [⊕]	122 [⊕]	105 [⊕]	17 [⊕]	3.257 [⊕]	3.543 [⊕]	1.14E-04 [⊕]	3.333 [⊕]	73.56 [⊕]	1.26E-04 [⊕]	10.5 [⊕]	6 [⊕]	3.323 [⊕]	77.02 [⊕]	1.30E-04 [⊕]	13.23 [⊕]	6 [⊕]
bkung16 [⊕]	130 [⊕]	71 [⊕]	59 [⊕]	1.968 [⊕]	2.034 [⊕]	1.42E-04 [⊕]	1.971 [⊕]	95.16 [⊕]	1.25E-04 [⊕]	-11.9 [⊕]	3 [⊕]	1.975 [⊕]	88.76 [⊕]	1.60E-04 [⊕]	12.61 [⊕]	3 [⊕]
c499 [⊕]	182 [⊕]	153 [⊕]	29 [⊕]	1.978 [⊕]	2.437 [⊕]	2.32E-04 [⊕]	2.322 [⊕]	25.04 [⊕]	2.16E-04 [⊕]	-6.94 [⊕]	17 [⊕]	2.287 [⊕]	32.64 [⊕]	2.32E-04 [⊕]	0.11 [⊕]	21 [⊕]
kogge16 [⊕]	199 [⊕]	76 [⊕]	123 [⊕]	1.319 [⊕]	1.41 [⊕]	2.07E-04 [⊕]	1.39 [⊕]	21.45 [⊕]	1.89E-04 [⊕]	-8.78 [⊕]	14 [⊕]	1.385 [⊕]	27.12 [⊕]	2.14E-04 [⊕]	3.43 [⊕]	16 [⊕]
log16 [⊕]	256 [⊕]	188 [⊕]	68 [⊕]	1.877 [⊕]	2.15 [⊕]	2.10E-04 [⊕]	2.083 [⊕]	24.34 [⊕]	2.18E-04 [⊕]	3.52 [⊕]	9 [⊕]	2.017 [⊕]	48.81 [⊕]	2.20E-04 [⊕]	4.74 [⊕]	2 [⊕]
bkung32 [⊕]	271 [⊕]	149 [⊕]	122 [⊕]	2.446 [⊕]	2.595 [⊕]	2.89E-04 [⊕]	2.48 [⊕]	77.43 [⊕]	2.70E-04 [⊕]	-6.57 [⊕]	5 [⊕]	2.477 [⊕]	79.31 [⊕]	3.30E-04 [⊕]	13.96 [⊕]	3 [⊕]
c432 [⊕]	297 [⊕]	277 [⊕]	20 [⊕]	4.993 [⊕]	5.411 [⊕]	2.43E-04 [⊕]	5.217 [⊕]	46.5 [⊕]	2.30E-04 [⊕]	-5.1 [⊕]	16 [⊕]	5.184 [⊕]	54.45 [⊕]	2.50E-04 [⊕]	3.1 [⊕]	8 [⊕]
array8x8 [⊕]	401 [⊕]	372 [⊕]	29 [⊕]	6.129 [⊕]	6.875 [⊕]	4.14E-04 [⊕]	6.479 [⊕]	53.12 [⊕]	4.14E-04 [⊕]	-0.01 [⊕]	7 [⊕]	6.457 [⊕]	56.12 [⊕]	4.40E-04 [⊕]	6.38 [⊕]	7 [⊕]
kogge32 [⊕]	487 [⊕]	155 [⊕]	332 [⊕]	1.569 [⊕]	1.782 [⊕]	4.72E-04 [⊕]	1.698 [⊕]	39.46 [⊕]	4.55E-04 [⊕]	-3.74 [⊕]	12 [⊕]	1.677 [⊕]	49.26 [⊕]	5.51E-04 [⊕]	16.75 [⊕]	10 [⊕]
pmult8x8 [⊕]	490 [⊕]	449 [⊕]	41 [⊕]	6.292 [⊕]	6.79 [⊕]	4.68E-04 [⊕]	6.429 [⊕]	72.46 [⊕]	4.60E-04 [⊕]	-1.54 [⊕]	4 [⊕]	6.379 [⊕]	82.44 [⊕]	5.28E-04 [⊕]	12.91 [⊕]	4 [⊕]
c880 [⊕]	535 [⊕]	175 [⊕]	360 [⊕]	3.386 [⊕]	3.794 [⊕]	3.96E-04 [⊕]	3.493 [⊕]	73.69 [⊕]	4.08E-04 [⊕]	3.01 [⊕]	7 [⊕]	3.475 [⊕]	78.2 [⊕]	5.68E-04 [⊕]	43.46 [⊕]	6 [⊕]
log32 [⊕]	640 [⊕]	444 [⊕]	196 [⊕]	3.531 [⊕]	4.273 [⊕]	5.23E-04 [⊕]	4.199 [⊕]	9.95 [⊕]	5.58E-04 [⊕]	6.74 [⊕]	19 [⊕]	4.126 [⊕]	19.79 [⊕]	9.81E-04 [⊕]	87.74 [⊕]	14 [⊕]
c1355 [⊕]	942 [⊕]	817 [⊕]	125 [⊕]	3.818 [⊕]	4.566 [⊕]	6.44E-04 [⊕]	4.301 [⊕]	35.41 [⊕]	6.84E-04 [⊕]	6.19 [⊕]	16 [⊕]	4.284 [⊕]	37.76 [⊕]	7.74E-04 [⊕]	20.15 [⊕]	12 [⊕]
c1908 [⊕]	977 [⊕]	566 [⊕]	411 [⊕]	4.576 [⊕]	5.293 [⊕]	6.72E-04 [⊕]	4.77 [⊕]	72.99 [⊕]	6.50E-04 [⊕]	-3.29 [⊕]	7 [⊕]	4.71 [⊕]	81.27 [⊕]	9.66E-04 [⊕]	43.82 [⊕]	5 [⊕]
c2670 [⊕]	1173 [⊕]	835 [⊕]	338 [⊕]	4.706 [⊕]	5.346 [⊕]	8.68E-04 [⊕]	5.001 [⊕]	53.97 [⊕]	8.46E-04 [⊕]	-2.51 [⊕]	5 [⊕]	5.001 [⊕]	54 [⊕]	1.35E-03 [⊕]	55.23 [⊕]	5 [⊕]
booth9x9 [⊕]	1206 [⊕]	1052 [⊕]	154 [⊕]	5.056 [⊕]	5.968 [⊕]	1.11E-03 [⊕]	5.468 [⊕]	54.87 [⊕]	1.15E-03 [⊕]	3.42 [⊕]	14 [⊕]	5.45 [⊕]	56.25 [⊕]	1.32E-03 [⊕]	18.61 [⊕]	6 [⊕]
log64 [⊕]	1536 [⊕]	1020 [⊕]	516 [⊕]	7.109 [⊕]	8.878 [⊕]	1.31E-03 [⊕]	8.571 [⊕]	17.37 [⊕]	1.30E-03 [⊕]	-1.25 [⊕]	22 [⊕]	8.526 [⊕]	19.88 [⊕]	2.36E-03 [⊕]	79.44 [⊕]	14 [⊕]
c3540 [⊕]	1743 [⊕]	1491 [⊕]	252 [⊕]	6.035 [⊕]	6.869 [⊕]	1.23E-03 [⊕]	6.414 [⊕]	54.6 [⊕]	1.30E-03 [⊕]	5.45 [⊕]	8 [⊕]	6.41 [⊕]	55.01 [⊕]	1.38E-03 [⊕]	12.11 [⊕]	9 [⊕]
pmult16x16 [⊕]	1934 [⊕]	1845 [⊕]	89 [⊕]	13.162 [⊕]	14.486 [⊕]	1.88E-03 [⊕]	13.517 [⊕]	73.2 [⊕]	1.90E-03 [⊕]	0.95 [⊕]	4 [⊕]	13.292 [⊕]	90.19 [⊕]	2.21E-03 [⊕]	17.32 [⊕]	4 [⊕]
c5315 [⊕]	2364 [⊕]	1074 [⊕]	1290 [⊕]	6.262 [⊕]	7.036 [⊕]	1.77E-03 [⊕]	6.563 [⊕]	61.16 [⊕]	1.54E-03 [⊕]	-12.83 [⊕]	4 [⊕]	6.454 [⊕]	75.23 [⊕]	2.38E-03 [⊕]	34.52 [⊕]	4 [⊕]
c7552 [⊕]	3912 [⊕]	414 [⊕]	3498 [⊕]	6.392 [⊕]	7.254 [⊕]	2.42E-03 [⊕]	6.614 [⊕]	74.21 [⊕]	1.88E-03 [⊕]	-22.05 [⊕]	6 [⊕]	6.605 [⊕]	75.34 [⊕]	6.03E-03 [⊕]	149.43 [⊕]	6 [⊕]
Gate#>1000 [⊕]	↔	55.7% [⊕]	44.3% [⊕]	↔	↔	↔	↔	55.63 [⊕]	↔	-4.12 [⊕]	9 [⊕]	↔	60.84 [⊕]	↔	52.38 [⊕]	6.86 [⊕]
average [⊕]	↔	59.4% [⊕]	40.6% [⊕]	↔	↔	↔	↔	52.98 [⊕]	↔	-2.5 [⊕]	9.63 [⊕]	↔	58.98 [⊕]	↔	29.96 [⊕]	7.77 [⊕]



Simulation Results-SVA(5)

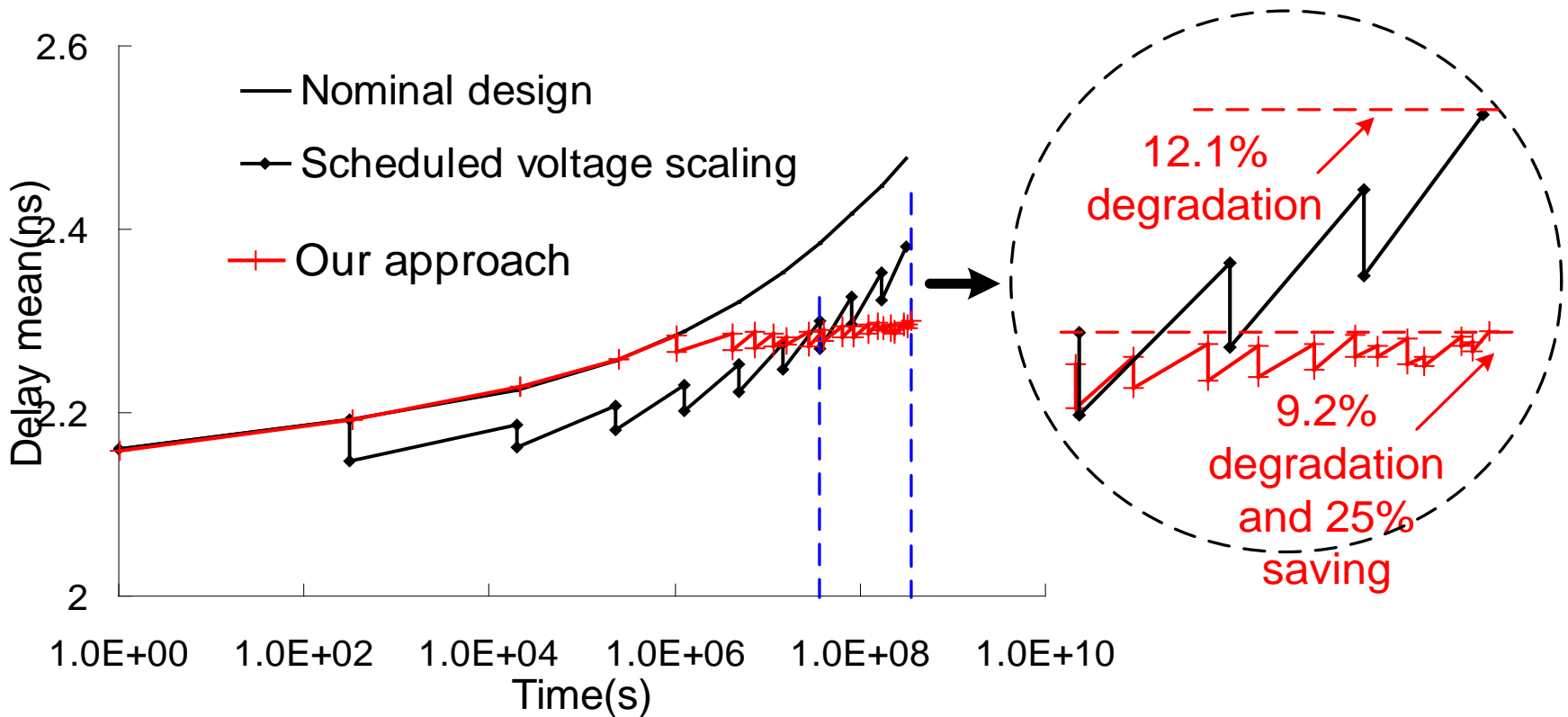
- Compare SVA with single Vdd dynamic scaling for c1908





Simulation Results-SVA(6)

- Compare scheduled technique [ASPDAC2009] with our SVA for c499





Simulation Results-SVA(7)

- Results of SVA technique on STA platform

circuit	$D_{imp}(\%)$	$L_{inc}(\%)$	Lv#
array4x4	76.58	-8.04	7
pmult4x4	57.97	-12.96	5
Bkung16	82.71	-10.52	1
c499	37.75	-8.95	18
Kogge16	39.41	-5.77	11
log16	61.54	-7.82	14
Bkung32	85.95	-19.20	4
c432	65.11	-7.09	11
array8x8	27.06	-9.16	21
Kogge32	50.81	-3.46	12
pmult8x8	60.16	-12.13	5
c880	50.42	-5.62	7
log32	32.71	-9.49	19
c1355	37.69	-6.02	19
c1908	78.83	-15.10	7
c2670	54.88	-17.26	4
booth9x9	45.24	-6.30	12
log64	33.19	-11.05	21
c3540	43.61	-4.97	10
pmult16x16	56.80	-11.19	6
c5315	88.39	-18.08	6
c7552	60.34	-26.10	5
Gate#>1000	54.64	-17.56	9.1
average	55.78	-10.74	10.2

$D_{imp}(\%)$	$L_{inc}(\%)$
55.78	-10.74
52.98	-2.5

STA

SSTA

STA model without considering variations underestimates the NBTI degradation and leakage.



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Conclusion

- Our SVA technique can mitigate on average 52.98% of NBTI degradation without increasing the maximum leakage power.
- Compared with the pure single Vdd dynamic scaling technique, we can reduce on average 32.46% more leakage power.
- For large circuits, there are more gates that can be assigned to low Vdd in LVS, so it has more space to reduce leakage power.
- Compared with scheduled voltage scaling technique [ASPDAC2009], our dynamic scaling technique is more effective because the circuit delay will exactly meet the specification at each dynamically decided time node during circuit operation.
- STA model without considering variations underestimates the NBTI-induced degradation and leakage power.



Thank you for your attention.

Q & A

谢谢

