Variation-Aware Supply Voltage Assignment for Minimizing Circuit Degradation and Leakage

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ABSTRACT

As technology scales, Negative Bias Temperature Instability (NBTI) has become a major reliability concern for circuit designers. And the growing process variations can no longer be ignored. Meanwhile, reducing leakage power remains to be one of the design goals. In this paper, we first present a platform for NBTI-aware statistical timing and leakage power analysis. A variation-aware supply voltage assignment (SVA) technique combining dual V_{dd} assignment and dynamic V_{dd} scaling techniques is proposed to minimize NBTI degradation and leakage. Based on the statistical platform, we analyze the impact of V_{th} variations on NBTI degradation and leakage. The experimental results show that our SVA technique can mitigate on average 52.98% of NBTI degradation with little or without leakage power increase; furthermore, it can reduce on average 32.46% more leakage power compared with the pure single V_{dd} scaling technique. Compared with scheduled voltage scaling technique [9], our dynamic scaling technique is more effective because the circuit delay will exactly meet the specification at each dynamically decided time node during circuit operation.

Categories and Subject Descriptors: J.6 [Computer Aided Engineering]: Computer aided design (CAD), B.6.3 [Design Aids]: Optimization.

General Terms: Algorithms, Design

Keywords: Negative Bias Temperature Instability (NBTI), leakage power, dual V_{dd}, dynamic V_{dd} scaling

1. INTRODUCTION

With the continuous scaling of CMOS technology, Negative Bias Temperature Instability (NBTI) is emerging as one of the major reliability degradation mechanisms [1]. NBTI is an aging effect which gradually increases the threshold voltage of PMOS transistors when they are negatively biased, thus leading to an increase of gate delay. Over a long period, such effect results in degradation in circuit speed. Moreover, the drastically growing process and device variations are emerging as key influencing factors of circuit performance. Traditional Static Timing Analysis (STA) is becoming insufficient to accurately evaluate the various variations' impact on circuit performance. Instead, Statistical Static Timing Analysis (SSTA) is an effective technique to evaluate the increasing variations [2].

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Meanwhile, leakage power has become a large portion of the total power consumption. During circuit operation time, NBTI-induced V_{th} degradation and process variations may severely affect the leakage power. The variations may cause the leakage magnitude and distribution to become larger and wider [3, 4]. So how to accurately analyze and reduce leakage power under the impact of both NBTI and variations needs to be solved.

Many researchers have explored how to mitigate NBTI degradation, and have provided some techniques such as synthesis [5], sizing [6], Input Vector Control(IVC) [7], and Internal Node Control(INC) [8]. These techniques are implemented at the design time and the circuit is fixed during the circuit operation time. However due to the various variations, the circuit performance may be changed during operation time and be different from the prediction results.

Recently a few adaptive techniques were proposed to mitigate the NBTI effect during the circuit operation. Zhang *et al*. [9] proposed a scheduled voltage scaling to increase lifetime. They gradually increase V_{dd} to compensate for NBTI degradation. Their technique has the potential to increase IC lifetime by 46% compared with guard-banding, while using 10 discrete voltage levels increase IC lifetime by 32.5%. However, their results were based on theoretic analysis. Scheduled technique is suitable for any circuits. Furthermore, they achieved a lower leakage power compared with guard-banding; in fact, leakage power will be significantly higher than the original value without any NBTI protection techniques. Kumar *et al*. [10] proposed an Adaptive Body Biasing(ABB) and Adaptive Supply Voltage(ASV) technique: they adjust the supply and bias voltage during circuit operation to recover the circuit performance. Their technique has a minimal overhead in area and a small increase in power compared with guard-banding. However, they still increased the leakage by 27% on average compared with the original value. Both Zhang and Kumar's results were based on deterministic performance estimation without considering variations.

In this paper, a variation-aware supply voltage assignment (SVA) technique combining dual V_{dd} assignment and dynamic V_{dd} scaling techniques is proposed based on a statistical platform to minimize NBTI degradation and leakage:

1) We build a statistical platform for statistical timing, NBTI and leakage analysis considering V_{th} variations.
2) We propose a variation-aware SVA technique.

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a) Dual V_{dd} is used instead of single scaling supply voltage.
b) During circuit operation, we dynamically adjust the time nodes at which the supply voltages need to be scaled. The optimal V_{dd} values are also dynamically determined according to the circuit performance.

3) The experimental results show that SVA technique can mitigate on average 52.98% of NBTI degradation without increasing the maximum leakage. Compared with pure single V_{dd} scaling, SVA technique can reduce 32.46% more leakage.

2. MODEL REVIEW

2.1 Gate delay and NBTI model

According to the alpha-power law, the load dependent delay of gate v is given by [11]:

$$D(v) = \frac{KC_L V_{dd}}{(V_{dd} - V_{th})^{\alpha}} \approx KC_L V_{dd}^{1-\alpha}\left(1 + \alpha \frac{V_{th}}{V_{dd}}\right) \quad (1)$$

where C_L is the load capacitance, K and α are constants.

NBTI can be described using Reaction-Diffusion mechanism [12-14]. When a PMOS transistor is negatively biased, the holes in the channel weaken the Si-H bonds, results in the generation of positive interface charges and hydrogen species, and then, threshold voltage of PMOS increases. The threshold voltage shifts ΔV_{th} under static NBTI can be calculated as [13,14]:

$$\Delta V_{th}(t) = \left(\frac{qT_{ox}}{\varepsilon_{ox}}\right)\sqrt[3]{k^2 C_{ox}\left(V_{gs} - V_{th}\right)\exp\left(\frac{2E_{ox}}{E_0}\right)(Ct)^{\frac{1}{6}}} \quad (2)$$

where q is the electron charge, k is the Boltzmann constant, C_{ox} is the oxide capacitance per unit area and $E_{ox}=(V_{gs}-V_{th})/T_{ox}$.

2.2 Leakage power model

A leakage lookup table is created by simulating all the standard cell types under all possible input patterns and varying V_{dd}, V_{th}. Thus the leakage power can be expressed as:

$$P_{leak} = V_{dd} \times \sum_{input} I_{leak}(v, input, V_{dd}, V_{th}) \times Prob(v, input) \quad (3)$$

where $I_{leak}(v,input,V_{dd},V_{th})$ and $Prob(v,input)$ are the leakage current and the probability of gate v under input pattern *input*. Leakage power will be smaller due to the NBTI degradation and be larger under high V_{dd} stress according to the formulas in [3, 15].

3. STATISTICAL ANALYSIS PLATFORM

3.1 Overview of the statistical flow

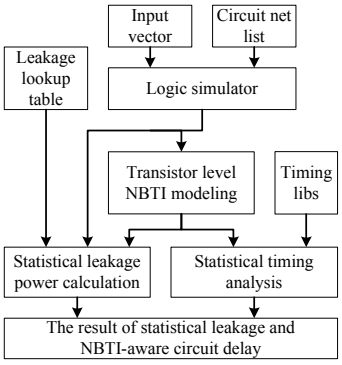

Figure 1. Our statistical NBTI and leakage analysis flow.

Figure 1 shows our statistical NBTI and leakage analysis flow. For a given circuit, logic simulator is used to generate the voltage level of each internal node. The NBTI-induced delay degradation of each gate at a given time node is calculated through transistor level NBTI model, and then the statistical timing of the circuit can be calculated. The leakage power is estimated through the input vector aware leakage lookup tables.

Table 1. The variables in the statistical algorithm.

variable	definition
V_i	Threshold voltage (V_{th}) of gate i
D_i	Delay of gate i considering NBTI degradation
AT_i	Arrival time at the input of gate i
LT_i	Leave time at the output of gate i
μ_x	The mean value of random variable x
σ_x	The standard deviation of random variable x

Algorithm 1: Statistical Timing Analysis Algorithm

Input: circuit net list, cell libraries, leakage lookup table, time t.
Output: $\mu_{LT}(t)$ and $\sigma_{LT}(t)$ at time t.

1. Calculate correlation coefficient of all the gates;
2. Calculate $\mu_{Vi}(t)$,$\sigma_{Vi}(t)$, $\mu_{Di}(t)$,$\sigma_{Di}(t)$ of each gate at time t;
3. for i=1 **to** n in topological order
4. **if** v_i is a primary input **then**
5. $\mu_{ATi}(t)$=0,$\sigma_{AT}(t)_i$=0;
6. **else** v_i is an internal gate **then**
7. Calculate$\mu_{ATi}(t)$ and$\sigma_{ATi}(t)$ using max operation;
8. Calculate $\mu_{LT}(t)_i$ and$\sigma_{LTi}(t)$ using add operation;
9. end for
10. Calculate$\mu_{LT}(t)$ and$\sigma_{LT}(t)$ of output;

Figure 2. The statistical timing analysis algorithm.

Table 1 shows the variables in the statistical timing analysis algorithm and figure 2 shows the algorithm. We first calculate the correlation coefficient of all the gates. Mean value and standard deviation of V_{th} at time t are calculated using the NBTI model. We evaluate all the gates in a topological order. If the gate is a primary input, then its mean value and standard deviation of arrival time are both set to be 0. Otherwise it's an internal gate, the arrival time is calculated using **MAX** operation considering all its inputs, then the leave time at its output is calculated by **ADD** operation. Finally we calculate the delay of the whole circuit. The total leakage power can be calculated as follows:

$$\mu_{leak}(t) = \sum_{i=1}^{N} \mu_{Li}(t) \quad (4)$$

$$\sigma_{leak}^2(t) = \sum_{i=1}^{N} \sigma_{Li}^2(t) + 2\sum_{i>j} \sigma_{Li}(t)\rho_{ij}\sigma_{Lj}(t)$$

Where $\mu_{Li}(t)$ and $\sigma_{Li}(t)$ are mean value and standard deviation of leakage power of gate i at time t.

3.2 Modeling of variation

Many variations strongly affect the gate delay. Since gate delay and leakage both strongly depend on V_{th}, we simply consider the V_{th} variations and assume that it is modeled by Gaussian distribution:

$$PDF(V_{th}) = \frac{1}{\sqrt{2\pi}\sigma_{th}} e^{-\frac{1}{2}\left(\frac{V_{th}-\mu_{th}}{\sigma_{th}}\right)^2} \quad (5)$$

3.3 Operations for timing analysis

1) **ADD** operation: Given mean value and variance of n gates in one path, mean value and variance of the path delay are calculated:

$$\mu = \sum_{i=1}^{n} \mu_i, \sigma^2 = \sum_{i=1}^{n}\sum_{j=1}^{n} \sigma_i \rho_{ij} \sigma_j \quad (6)$$

2) **MAX** operation: In many cases, the MAX result of two or more Gaussian distribution can be assumed as an approximate Gaussian distribution [16], the mean value and standard deviation are calculated with Clark's formula [17]:

$$\mu = \mu_1\Phi(\alpha) + \mu_2\Phi(-\alpha) + a\varphi(\alpha) \quad (7)$$
$$\sigma^2 = (\mu_1^2 + \sigma_1^2)\Phi(\alpha) + (\mu_2^2 + \sigma_2^2)\Phi(-\alpha) + (\mu_1 + \mu_2)a\varphi(\alpha) - \mu^2$$

where

$$\alpha = \frac{\mu_1 - \mu_2}{\sqrt{\sigma_1^2 + \sigma_2^2 - 2\sigma_1\sigma_2\rho}} \quad (8)$$

3.4 Correlation coefficient of all the gates

We assume that the logically close gates are also spatially close, and the threshold voltage of gate v_i is correlated with some nearest gates, each correlation coefficient is:

$$\rho(v_i, v_{i\pm k}) = \rho_k \ (\rho_i > \rho_j \ \textit{for any} \ i < j) \quad (9)$$

The threshold voltage of each gate v_i is expressed as linear combinations of its mean value and random variables:

$$V_{i,th} = V_i + a_0\Delta V_i + \sum_{j=1}^{n} a_j \Delta V_{i+j} + \sum_{j=1}^{n} a_j \Delta V_{i-j} \quad (10)$$

where ΔV_i's are standard Gaussian random variables; V_i is the mean value of $V_{i,th}$. We can get ρ_i's from lab measurement, a_i's can be calculated as:

$$\rho_k = \frac{2a_0a_k + 2\sum_{i=1}^{n-k} a_i a_{i+k} + \sum_{i+j=k, i\geq 1, j\geq 1} a_i a_j}{a_0^2 + 2\sum_{i=1}^{n} a_i^2} \quad (11)$$

4. SUPPLY VOLTAGE ASSIGNMENT(SVA)

4.1 Overview of the SVA technique

Based on the NBTI model, gate V_{th} will increase and then results in degradation in circuit speed. To counteract the degradation, V_{dd} must gradually increase. However, increasing V_{dd} will directly increase leakage. We notice that it is not necessary to increase all gates' V_{dd}, because non-critical gates have delay slack. So instead of using one scaling supply voltage, we propose to use dual V_{dd}, the high V_{dd} is used to compensate for NBTI degradation on critical gates, while low V_{dd} is used to reduce leakage power on other gates who do not affect the circuit delay. Furthermore, In our technique, all the protection parameters are dynamically calculated according to the circuit performance constraints.

Algorithm 2: Dual V_{dd} and dynamic V_{dd} scaling algorithm

Input: circuit net list, cell libraries, leakage lookup table.

Output: voltage level number n, time nodes t_0=0,t_1,…,t_n, V_{ddhigh}, V_{ddlow}, leakage power (mean and standard deviation), NBTI-aware delay (mean and standard deviation) at all time nodes t_0,…,t_n.

1. Calculate the nominal delay and leakage and then determine HVS (high V_{dd} set) and LVS (low V_{dd} set);

2. do
3. Calculate all the statistical delay and leakage at time t_i;
4. *Determine the optimal high voltage $V_{ddhigh}(t_{i+1})$ for mitigating NBTI-induced degradation*;
5. *Determine the optimal low voltage $V_{ddlow}(t_{i+1})$ for leakage power reduction*;
6. Update V_{dd} and estimate V_{th} degradation of each gate;
7. Predict the next time node t_{i+1};
8. i++;
9. while time node doesn't achieve the circuit lifetime.

Figure 3. The variation-aware SVA algorithm.

There are two steps in our technique(Fig. 3): 1) Dual V_{dd} assignment: divide all the gates into two sets: **HVS (high V_{dd} set)** and **LVS (low V_{dd} set)**; 2) Dynamic V_{dd} scaling: dynamically determine the optimal time nodes and the voltage values.

4.2 Dual V_{dd} assignment

In the beginning, the nominal delay and leakage power at time 0 are calculated. Then we determine two gate sets: HVS (high V_{dd} set) and LVS (low V_{dd} set). Since a low V_{dd} gate cannot directly drive a high V_{dd} gate, a level converter should be used. In order to avoid level converters, HVS includes all the critical gates and all the predecessors of critical gates; LVS is composed of all the rest gates who do not directly affect the circuit delay. Generally speaking, HVS is larger than LVS for most circuits. Based on the proportion between HVS and LVS of each circuit, we can approximately estimate the potential of NBTI-induced degradation mitigation and leakage reduction by our technique.

4.3 Dynamic V_{dd} scaling

In our technique, we set a delay specification for each circuit, which is chosen as the delay value of each circuit when t=10 days.

At time 0, we first calculate mean value and standard deviation of delay and leakage, then determine the optimal $V_{ddhigh}(t_1)$ and $V_{ddlow}(t_1)$ which will be assigned in the following time interval $[t_0, t_1]$. The HVS gates are assigned V_{ddhigh} while LVS gates are assigned V_{ddlow}. The detailed determination of V_{ddhigh} and V_{ddlow} will be described in the below. With new $V_{ddhigh}(t_1)$ and $V_{ddlow}(t_1)$, we can estimate V_{th} degradation of each gate at later time as same as the method in [9], and then predict the next time node t_1 at which the circuit delay will exceed the specification and we need to scale supply voltages again.

The same procedure including three operations: determine optimal $V_{ddhigh}(t_{i+1})$, $V_{ddlow}(t_{i+1})$ and predict the next time node t_{i+1}, will be repeated at each time node t_i, until circuit lifetime ends.

4.3.1 Determine the optimal V_{ddhigh}

Figure 4 shows how V_{dd} scaling improves the delay degradation, the delay will be a sudden drop at time t_i immediately after assigning the optimal $V_{ddhigh}(t_{i+1})$. Notice that the higher $V_{ddhigh}(t_{i+1})$ is, the smaller the circuit delay at time t_i will be. However, higher V_{dd} leads to higher NBTI-induced V_{th} degradation and higher leakage power. Our object is to make sure that the circuit delay during time interval $[t_i, t_{i+1}]$ and leakage power at time t_i (leakage at t_i is the maximum value during $[t_i, t_{i+1}]$) achieve optimal values simultaneously. Considering statistical model, the object is to minimize the following function:

$$F = A\times\left(\mu_{D(t_{i+1})} + 3\sigma_{D(t_{i+1})}\right) + B\times\left(\mu_{L(t_i)} + 3\sigma_{L(t_i)}\right) \quad (12)$$

where A and B are two weight constants to balance the leakage and circuit delay, $D(t_{i+1})$ and $L(t_i)$ are the circuit delay at t_{i+1} and circuit leakage power at t_i. However, before $V_{ddhigh}(t_{i+1})$ is calculated we can't predict t_{i+1}, because t_{i+1} depends on $V_{ddhigh}(t_{i+1})$ which in turn depends on t_{i+1}. We simply assume that t_{i+1} equals to t_i+(t_i-t_{i-1}) (this assumption is only used in equation (12) to simply find the optimal V_{ddhigh}; after V_{ddhigh} is calculated, the real t_{i+1} will be predicted using NBTI degradation model). An approximate numerical algorithm is implemented to find the minimum value of equation (12) and corresponding V_{ddhigh}.

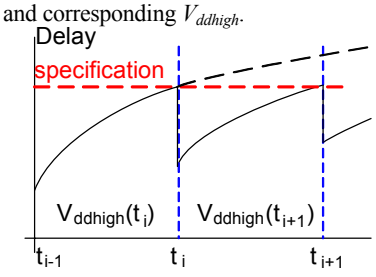

Figure 4. Impact of V_{dd} scaling on delay degradation.

4.3.2 Determine the optimal V_{ddlow}

Consider the gates in LVS, they have delay slack, so their delay can be relaxed and then their V_{dd}'s could be lower:

$$D_{relax}(v) = D_{current}(v) + C \times D_{slack}(v) \quad (13)$$

where D_{relax}, $D_{current}$, D_{slack} are the relaxed delay, the current delay, the delay slack of the gate v respectively. C is a constant between 0 and 1 to make sure that the gate in LVS will not change to be a critical one. With the relaxed gate delay and according to equation (1), the low V_{dd} of gate v denoted by $V_{ddlow}(v)$ can be calculated. The optimal V_{ddlow} of the whole circuit is the maximum value of all the V_{ddlow}'s.

4.4 Overhead of our technique

Dynamic V_{dd} scaling technique needs voltage regulator and DAC[9]. The detailed analysis of this overhead will not be discussed in this paper. On the other hand, we do not use level converters. Because besides critical gates, HVS also includes all the predecessors of critical gates, which may not be critical gates at all. In fact, these gates still have delay slack. So if we use level converters then the trade-off between leakage power and penalty induced by level converters must be well balanced.

5. SIMULATION RESULTS

5.1 Implementation and Experiment Setup

Our platform and algorithms are implemented by C++. The benchmark circuits are synthesized using a 65nm library from industry. Some key technology parameters are: nominal $|V_{dd}|$=1.0V; $|V_{th}|$=0.20V for both NMOS and PMOS transistors; T_{ox}=1.2nm. ISCAS85 benchmark and some ALU circuits are used to evaluate our platform and algorithms. The temperature is set to be 378K corresponding to the worst-case NBTI degradation and leakage. The circuit lifetime is set to be 10 years.

5.2 Impact of variations on NBTI and leakage

Figure 5 shows the impact of the V_{th} variations on NBTI for c880. The mean value of circuit delay considering variations is larger than the nominal value without variations. The delay distribution is the lower and upper bounds(μ±3σ). As time passing, the mean value increases due to NBTI effect, while the distribution becomes narrower which matches the silicon results in [12]. Figure 6 shows the impact of the V_{th} variations on leakage. The leakage decreases due to V_{th} shifts which is opposite compared with circuit delay degradation. Similar to NBTI, the mean value of leakage considering variations is larger than the nominal value and the leakage distribution becomes narrower.

Figure 7 shows our statistical timing results compared with Monte Carlo simulation for c880 results at 3 time nodes: 0, 3 years, and 10 years. It also shows that the mean value of delay increases and standard deviation decreases as the same as figure 5. Considering NBTI degradation, the lower bound (μ-3σ) of delay after 3 years is larger than the upper bound (μ+3σ) of delay at time 0. So NBTI is a major reliability degradation mechanism and can not be ignored in circuit estimation and optimization. Comparing our statistical timing results with Monte Carlo of all the circuits, the error ratio of the mean value of circuit delay is 0.98% on average and error ratio of standard deviation is 7.48% on average.

Runtime: our statistical platform is at least 5X faster (from 0.016s to 307s for benchmark circuits from array4x4 to C7552) than Monte Carlo method (from 16s to 1542s for benchmark circuits from array4x4 to C7552).

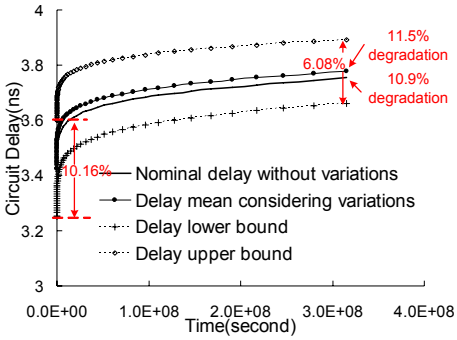

Figure 5. The impact of variations on NBTI for c880.

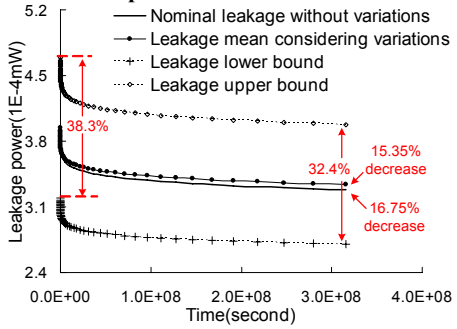

Figure 6. The impact of variations on leakage power for c880.

5.3 Results of variation-aware SVA technique

5.3.1 The effect of our technique

Figure 8 and 9 show how our technique is performed on c1908. In the beginning, our technique gets the same circuit delay as the nominal delay, because the delay does not achieve the specification. Once the delay exceeds the specification, the dual V_{dd} voltages are scaled, so the circuit delay has a sudden drop and leakage also has a sudden change. During circuit operates, the same procedure will be repeated at each time node to guarantee that the circuit delay does not exceed the specification and the leakage power reduces as much as possible. By increasing high V_{dd}, the delay by our technique is always smaller than the nominal degradation value. For c1908, we get 72.99% NBTI degradation saving compared with nominal design.

Figure 9 shows the leakage power reduction. The leakage power increases gradually because we increase the high V_{dd} at HVS gates which are more than gates in LVS for c1908. During early operation time, our technique can get a lower leakage power; while during later time, the leakage power increases and is larger than the nominal value. However, our dual V_{dd} technique can make the leakage power as low as possible and get 3.29% reduction of the maximum leakage power for c1908.

Figure 10 shows the V_{dd} scaling for c1908. The high V_{dd} increases to counteract the NBTI degradation, while the low V_{dd} decreases to reduce leakage. However it's not true for any circuits, because the NBTI effect will change the circuit timing during circuit operation, and the slack of each gate may severely change. Figure 11 shows the V_{dd} scaling for c7552. The high V_{dd} increases but low V_{dd} increases and decreases iteratively.

Figure 12 shows the comparison between single V_{dd} scaling technique and our dual V_{dd} scaling technique. By single V_{dd} scaling, we only use single high V_{dd} for all gates and scaling the V_{dd} to mitigate the NBTI degradation (similar but not same as [9] or [10]). During the whole circuit lifetime, the delay of our approach is very

close to that of single V_{dd} scaling technique. However, our approach can save 47% more leakage power than pure single V_{dd} scaling for c1908.

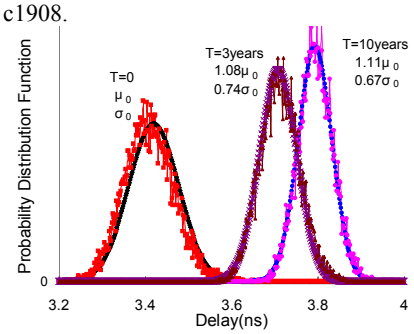

Figure 7. Delay distribution compared toMonte Carlo (C880)

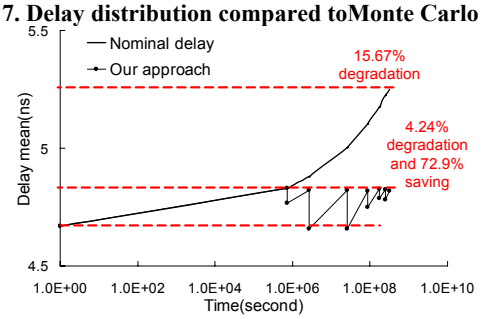

Figure 8. Delay improvement by SVA for c1908.

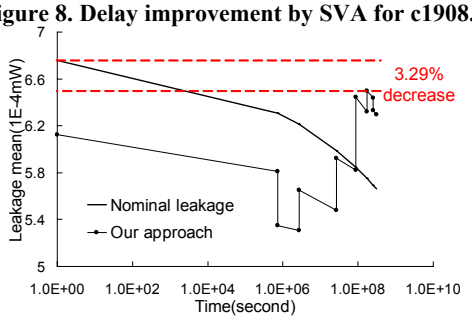

Figure 9. Leakage improvement by SVA for c1908.

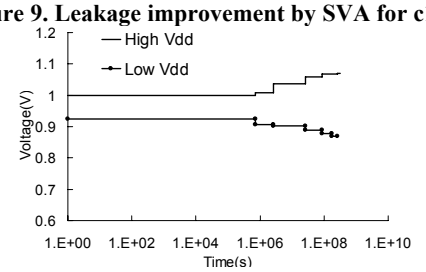

Figure 10. The voltage scaling for c1908.

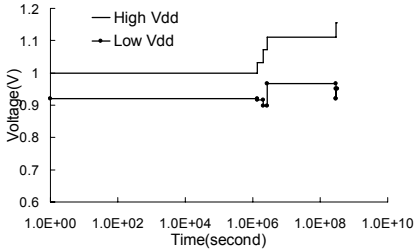

Figure 11. The voltage scaling for c7552.

Table 2 shows the detailed results of our SVA compared with pure single V_{dd} scaling. Column 5 (D_0) is the intrinsic circuit delay at time 0; columns 6 and 7 (D_{life}, L_0) are the mean value of maximum delay (after 10 years) and mean value of maximum leakage (at time 0) by nominal design; column 8 (D_{imp}) is the delay improvement and column 9 (L_{inc}) is the leakage increase by our approach; column 10 (Lv#) is the voltage level number. Columns 11-13 are the same meaning as columns 8-10 by single V_{dd} scaling technique.

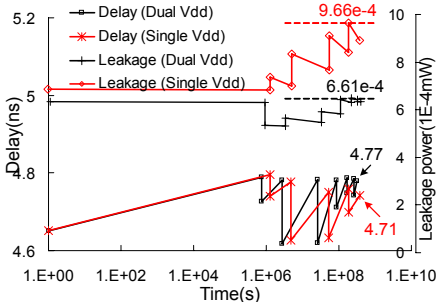

Figure 12. Compare SVA with single V_{dd} scaling for c1908.

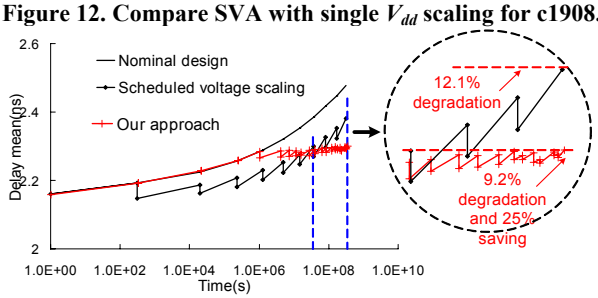

Figure 13. Compare scheduled technique with our SVA.

Table 3. Results of SVA technique on STA platform

circuit	D_{imp}(%)	L_{inc}(%)	Lv#
array4x4	76.58	-8.04	7
pmult4x4	57.97	-12.96	5
Bkung16	82.71	-10.52	1
c499	37.75	-8.95	18
Kogge16	39.41	-5.77	11
log16	61.54	-7.82	14
Bkung32	85.95	-19.20	4
c432	65.11	-7.09	11
array8x8	27.06	-9.16	21
Kogge32	50.81	-3.46	12
pmult8x8	60.16	-12.13	5
c880	50.42	-5.62	7
log32	32.71	-9.49	19
c1355	37.69	-6.02	19
c1908	78.83	-15.10	7
c2670	54.88	-17.26	4
booth9x9	45.24	-6.30	12
log64	33.19	-11.05	21
c3540	43.61	-4.97	10
pmult16x16	56.80	-11.19	6
c5315	88.39	-18.08	6
c7552	60.34	-26.10	5
Gate#>1000	54.64	-13.56	9.1
average	55.78	-10.74	10.2

The results show that SVA technique can mitigate on average 52.98% of NBTI degradation and save 2.5% of maximum leakage simultaneously. On the contrary, for single V_{dd} scaling, it only save 6% more delay degradation, however it causes 29.96% leakage increase. We also compare the results of large circuits with average results. For large circuits, the LVS gates number is more than that of average, hence more leakage saving can be achieved by our approach. Compared with single V_{dd} scaling, our technique can reduce 56.5% more leakage for large circuits. Furthermore, for different circuits, the voltage level, the time nodes and optimal voltage values are different. The average of voltage levels is 9.6, which is close to the optimal level number analyzed in [9]. However

scheduled voltage values and scheduled time nodes are not the optimal solution for any circuits. Figure 13 shows the results for c499, using 10 voltage levels and 10 time nodes chosen same as [9]. The comparison shows that scheduled technique adjusts too frequently in the beginning but less frequently during the later time, so it can't guarantee that the delay will not exceed a specification during circuit operation time.

Runtime: the runtime of our SVA ranges from 0.078s to 621s for the benchmark circuits array4x4 to C7552.

5.3.2 The impact of variations on results

We also implement our technique on STA platform without considering V_{th} variations. Table 3 shows the results implemented on STA platform. Compared with the results of SSTA, the STA results are better. STA results save 2.8% more NBTI degradation and reduce 8.24% more leakage power. The comparison shows that STA model without considering variations underestimates the NBTI degradation and leakage, which may be severely affected by variations (figure 5 and 6). So in order to get a more accurate optimization, SSTA is recommended.

6. CONCLUSION

Power and reliability have become two key design goals with technology scales. Meanwhile, the growing variations can severely affect circuit delay and leakage. In this paper, a supply voltage assignment technique combining dual V_{dd} and dynamic V_{dd} scaling is proposed on a statistical platform to minimize circuit degradation and leakage. Our technique can save on average 52.98% NBTI degradation and reduce 2.5% leakage; while for large circuits, we can save more leakage. Compared with single V_{dd} scaling, our technique save 32.46% more leakage on average. Furthermore, our technique is more flexible since the optimal results are dynamically decided for any circuits so that the circuit delay will exactly meet the specification at each time node during circuit operation.

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Table 2. The results of our SVA and comparison with single V_{dd} scaling

circuit	Gate#	HVS#	LVS#	Nominal design			Our SVA			Single V_{dd} scaling		
				D_0	D_{life}	L_0	D_{imp}(%)	L_{inc}(%)	Lv#	D_{imp}(%)	L_{inc}(%)	Lv#
array4x4	89	76	13	2.485	2.737	9.12E-05	55.51	-9.96	7	58.78	10.03	6
pmult4x4	122	105	17	3.257	3.543	1.14E-04	73.56	10.5	6	77.02	13.23	6
bkung16	130	71	59	1.968	2.034	1.42E-04	95.16	-11.9	3	88.76	12.61	3
c499	182	153	29	1.978	2.437	2.32E-04	25.04	-6.94	17	32.64	0.11	21
kogge16	199	76	123	1.319	1.41	2.07E-04	21.45	-8.78	14	27.12	3.43	16
log16	256	188	68	1.877	2.15	2.10E-04	24.34	3.52	9	48.81	4.74	2
bkung32	271	149	122	2.446	2.595	2.89E-04	77.43	-6.57	5	79.31	13.96	3
c432	297	277	20	4.993	5.411	2.43E-04	46.5	-5.1	16	54.45	3.1	8
array8x8	401	372	29	6.129	6.875	4.14E-04	53.12	-0.01	7	56.12	6.38	7
kogge32	487	155	332	1.569	1.782	4.72E-04	39.46	-3.74	12	49.26	16.75	10
pmult8x8	490	449	41	6.292	6.79	4.68E-04	72.46	-1.54	4	82.44	12.91	4
c880	535	175	360	3.386	3.794	3.96E-04	73.69	3.01	7	78.2	43.46	6
log32	640	444	196	3.531	4.273	5.23E-04	9.95	6.74	19	19.79	87.74	14
c1355	942	817	125	3.818	4.566	6.44E-04	35.41	6.19	16	37.76	20.15	12
c1908	977	566	411	4.576	5.293	6.72E-04	72.99	-3.29	7	81.27	43.82	5
c2670	1173	835	338	4.706	5.346	8.68E-04	53.97	-2.51	5	54	55.23	5
booth9x9	1206	1052	154	5.056	5.968	1.11E-03	54.87	3.42	14	56.25	18.61	6
log64	1536	1020	516	7.109	8.878	1.31E-03	17.37	-1.25	22	19.88	79.44	14
c3540	1743	1491	252	6.035	6.869	1.23E-03	54.6	5.45	8	55.01	12.11	9
pmult16x16	1934	1845	89	13.162	14.486	1.88E-03	73.2	0.95	4	90.19	17.32	4
c5315	2364	1074	1290	6.262	7.036	1.77E-03	61.16	-12.83	4	75.23	34.53	4
c7552	3912	414	3498	6.392	7.254	2.42E-03	74.21	-22.05	6	75.34	149.43	6
Gate#>1000		55.7%	44.3%				55.63	-4.12	9	60.84	52.38	6.86
average		59.4%	40.6%				52.98	-2.5	9.63	58.98	29.96	7.77