Gate Replacement Techniques for Simultaneous Leakage and Aging Optimization

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Outline

- Background
- Internal Node Control
- Gate Replacement
- NBTI/leakage Optimization Platform
- Simulation Results
- Conclusion

Background: Leakage

- **The circuit total power（P_{total}）can be calculated as：**

$$P_{total} = \underbrace{P_{switch} + P_{shortcircuit}}_{dynamic\ \ power} + \underbrace{P_{leakage}}_{static\ \ power}$$

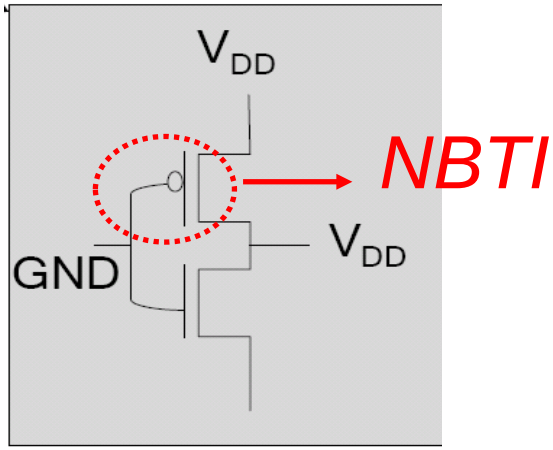
- **As technology scales, the dynamic power of one transistor decreases, while leakage power increases.**
- **Leakage is more than 50% of the total power. The modeling and optimization has been studied for 10 years or more.**

Leakage reduction techniques

- Standby time techniques
  - Power Gating
  - Input Vector Control
  - Body biasing → adapt Vth during the standby time
  - Adapt Vdd during the standby time
- Run time techniques
  - DVTS dynamic Vth scaling
  - DVS dynamic Vdd scaling
- Design time techniques
  - Dual Vth
  - Dual Vdd
  - Gate sizing
  - …

Background: Aging due to NBTI

- Negative Bias Temperature Instability
- Conditions
  - PMOS transistor
  - Negatively biased
  - elevated temperature



- Impact of NBTI on circuit performance
  - a shift in threshold voltage
  - a signifcant increase in the delay of PMOS devices, and result in about 10-20% degradation in circuit speed

NBTI mitigation techniques

- **Lower temperature, Vdd, and signal probability [DAC06]**
- **NBTI-aware Sizing [DATE06]**
- **NBTI-aware Synthesis [DAC07]**
- **Guard banding [ASPDAC08]**
- **Dynamic Adjustment (Vdd, Vth) [ASPDAC09]**
- **Input Vector control [DATE 07, MICRO 07]**
- **Memory NBTI mitigation [ISQED06]**
- **…**

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Input dependency of NBTI and leakage

- Both depend on the input
- For NBTI
  - 1 is the best
  - 0 is the worst

TABLE II

LEAKAGE POWER COMPARISON UNDER DIFFERENT INPUT VECTORS(65NM): A) NOR2 B) NAND3 C) INV. THE TEMPERATURE OF LEAKAGE POWER ESTIMATION IS SET TO 378K, $V_{dd} = 1V$.

A) NOR2

Input	Leakage(pW)
00	617.0
01	283.2
10	230.1
11	45.8

B) NAND3

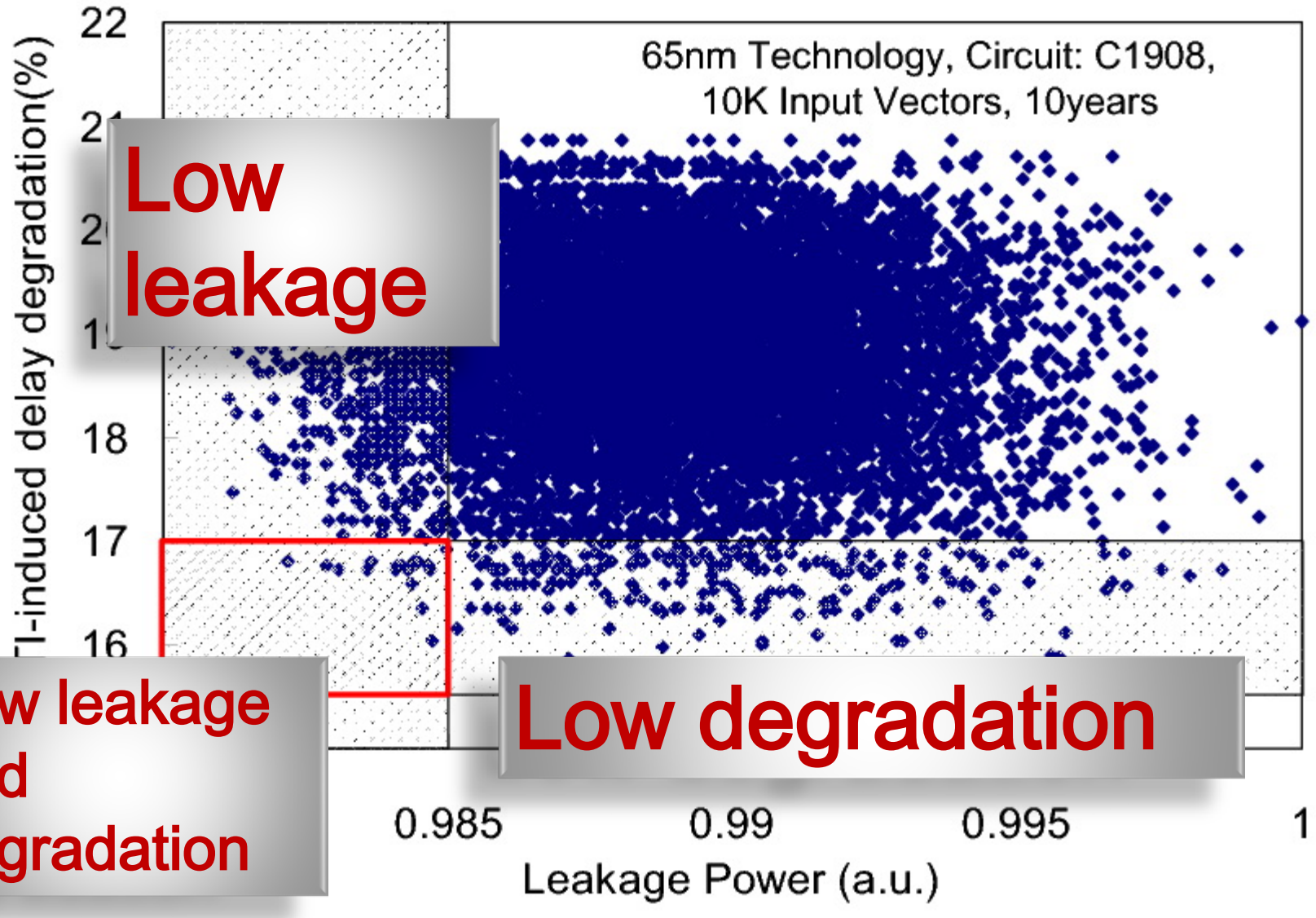
Input	Leakage(pW)
000	30.1
001	54.9
010	54.7
011	249.1
100	55.1
101	259.2
110	309.8
111	703.3

C) INV

Input	Leakage (pW)
0	633.2
1	791.3

- For Leakage, it is not the same story
  - the best case input patterns to mitigate the leakage for NAND/AND/INV gates are all 0's at the inputs
  - for NOR/OR/BUF gates are all 1's at the inputs.
- That is why we may get a trade off between leakage and NBTI

Input dependency of NBTI and leakage

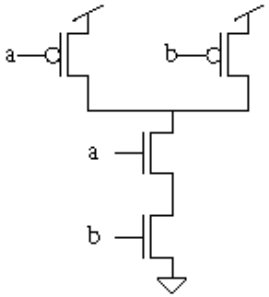


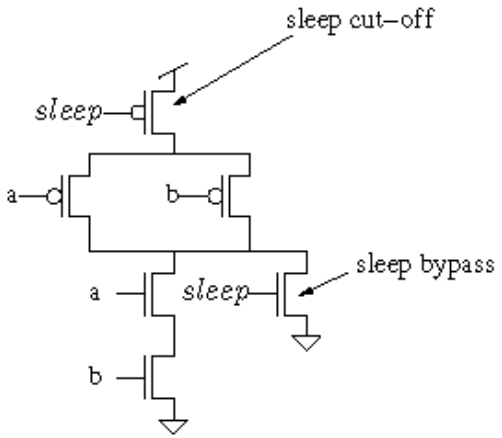
Why Internal Node Control ?

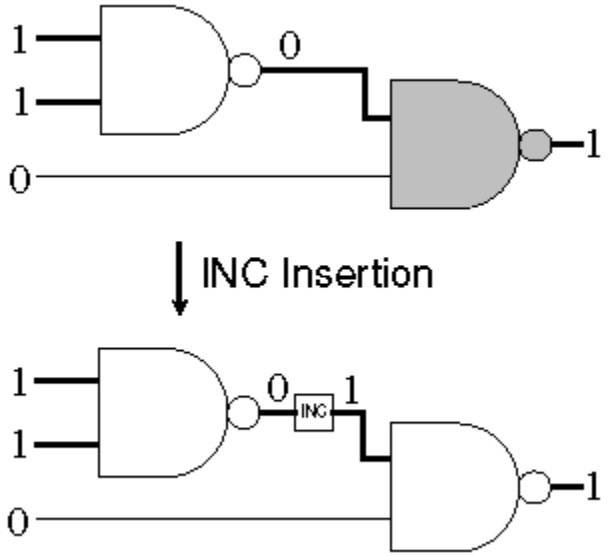
- We need to find the optimal input vectors for low leakage and degradation
- IVC?
  - Finding the optimal Input Vector is time consuming
  - The effect of IVC will be diminished when the circuit becomes larger
  - INC can control more internal gates in the circuit

Internal Node Control for Leakage

- **Gate Replacement**
  - **DAC 2005,2006**
- **Control Point Insertion**
  - **TCASII**
- **Sleep transistor insertion**
  - **DATE 2007**

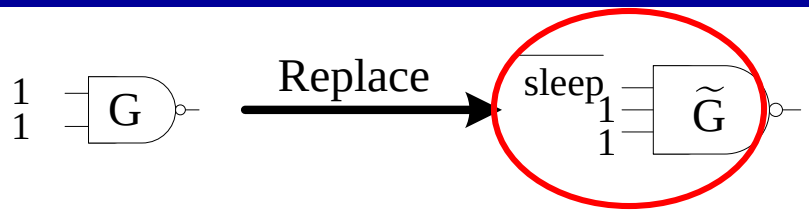


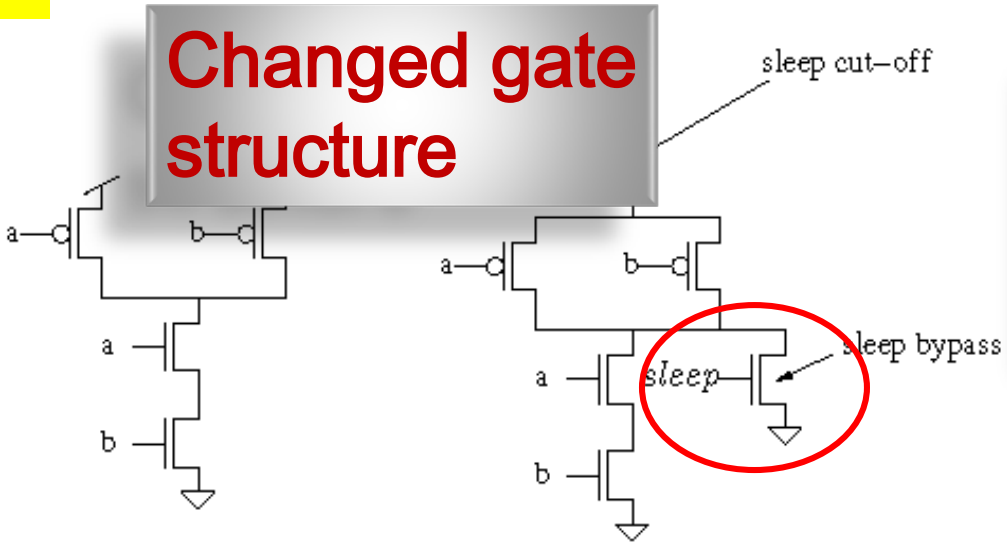


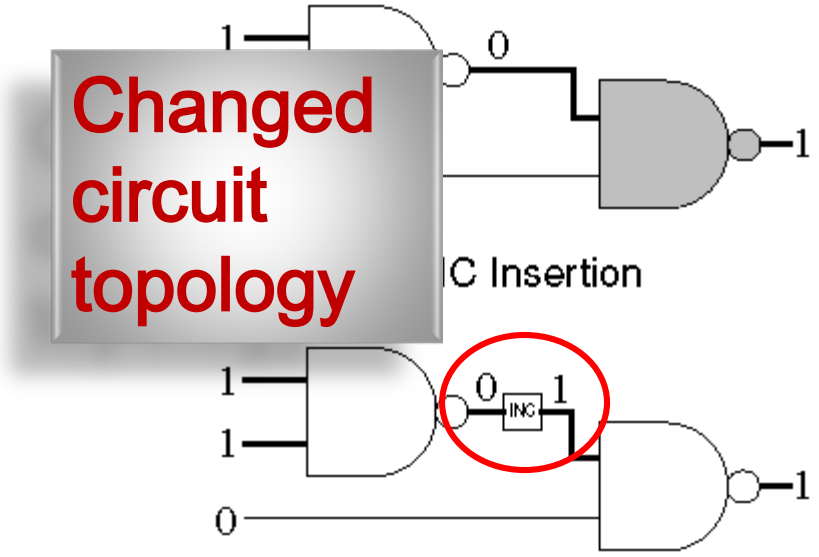


Why we choose gate replacement

- **Gate Replacement**
  - **Topology not changed**
  - **Gate structure not changed**
  - **Standard library can be directly used**







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Gate Replacement

- $G(\vec{x}) \xrightarrow{Replacement} \widetilde{G}(\vec{x}, sleep)$

- **When circuit is active(sleep=0)**

$$\widetilde{G}(\vec{x}, 0) = G(\vec{x})$$

- **When circuit is standby(sleep=1)**

$\widetilde{G}(\vec{x}, 1)$ **has smaller leakage power or can serve as an internal node control (INC) point to mitigate NBTI effect**

Gate Replacement

- **For Leakage**

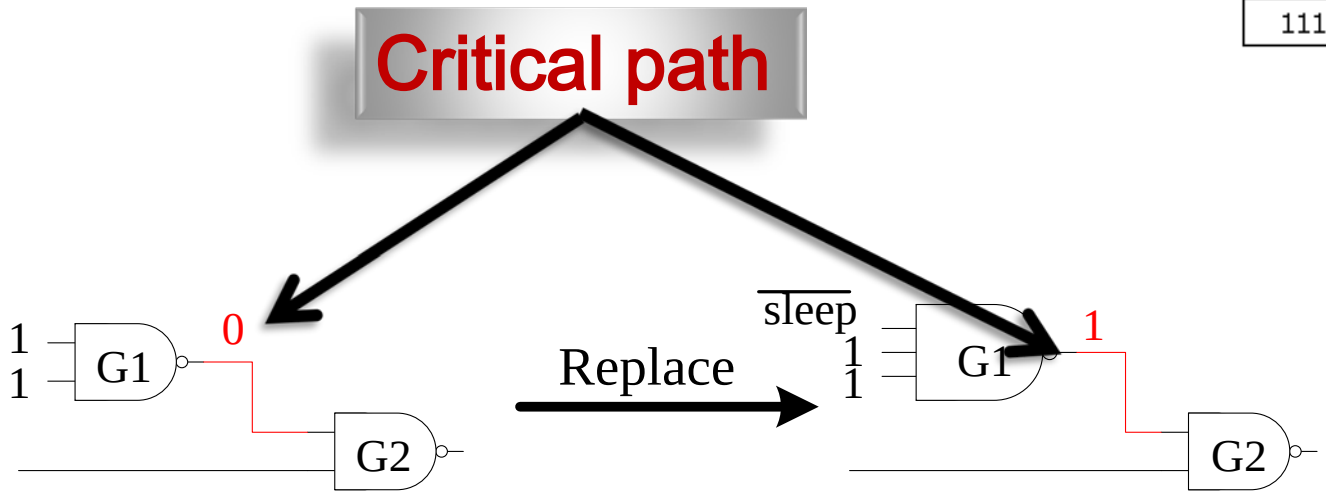
NAND2

Input	Leakage (pW)
00	54.4
01	257.7
10	309.0
11	454.7

NAND3

Input	Leakage (pW)
000	30.1
001	54.9
010	54.7
011	249.1
100	55.1
101	259.2
110	309.8
111	703.3

- **For NBTI**



Two Gate Replacement algorithms

- **Direct Gate Replacement Algorithm(DGR)**
  - L.Yuan and G.Qu, “A combined gate replacement and input vector control approach for leakage current reduction,”TVLSI2006
- **Divide and Conquer Based Gate Replacement Algorithm(DCBGR)**
  - L.Cheng, L.Deng, D.Chen, and M.Wong, “A fast simultaneous input vector generation and gate replacement algorithm for leakage power reduction,”DAC2006

Direct Gate Replacement

- **First Step:**
  - **Get an optimal input vector: an optimal input vector is chosen from 10K random input vector search, the object function is as follows**

$$F(D_{circuit}, P_{leakage}) = A \times D_{circuit} + B \times P_{leakage}$$

- **Second Step: Direct Gate Replacement based on the optimal input vector:**
  - **NBTI mitigation in the critical paths**
  - **Leakage power reduction in other paths**

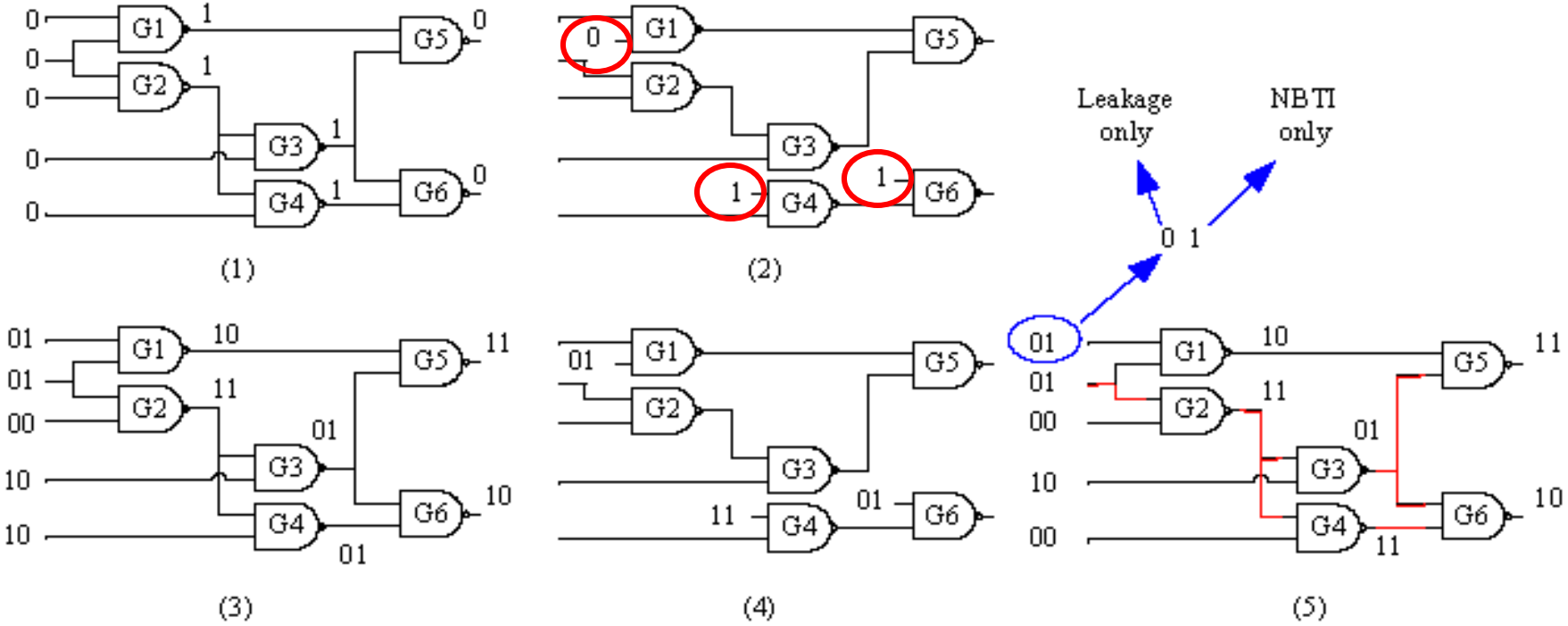
Divide-and-Conquer Based Gate Replacement Algorithm

- **Why we need DCBGR ?**
  - **The random input vector phase of DGR costs lots of time**
  - **The complexity of DGR is O(n^2)**
  - **DGR algorithm is based on an optimal input vector, it's local optimization but not global optimization.**

Divide-and-Conquer Based Gate Replacement Algorithm

- Divide the circuit into trees
- Gate replacement for each tree circuit
  - NBTI mitigation in the critical paths
  - Leakage power reduction in other paths
- Perform the algorithm on each tree circuit until it converges

An example for C17



DCBGR RESULTS FOR C17 CIRCUIT.

Object function	$D_O(ns)$	$D_{nbti}(ns)$	Degradation	LK(mW)
Leakage only	0.0796	0.0866	8.79%	1.44E-6
NBTI only	0.0796	0.0804	1%	2.09E-6

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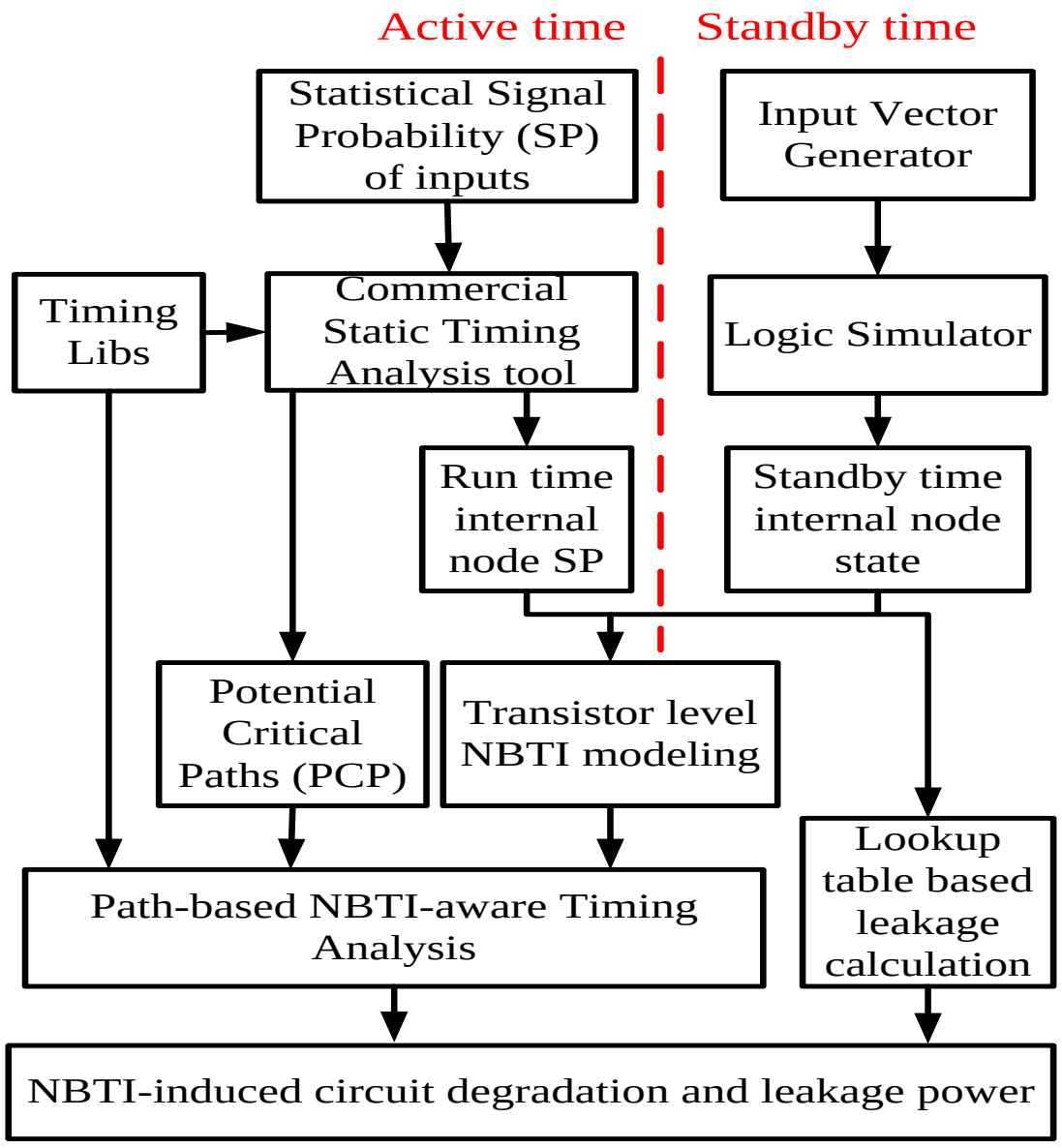
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Standby time
Statistical Signal Probability (SP) of inputs
Input Vector Generator
Timing Libs
Commercial Static Timing Analysis tool
Logic Simulator
Run time internal node SP
Standby time internal node state
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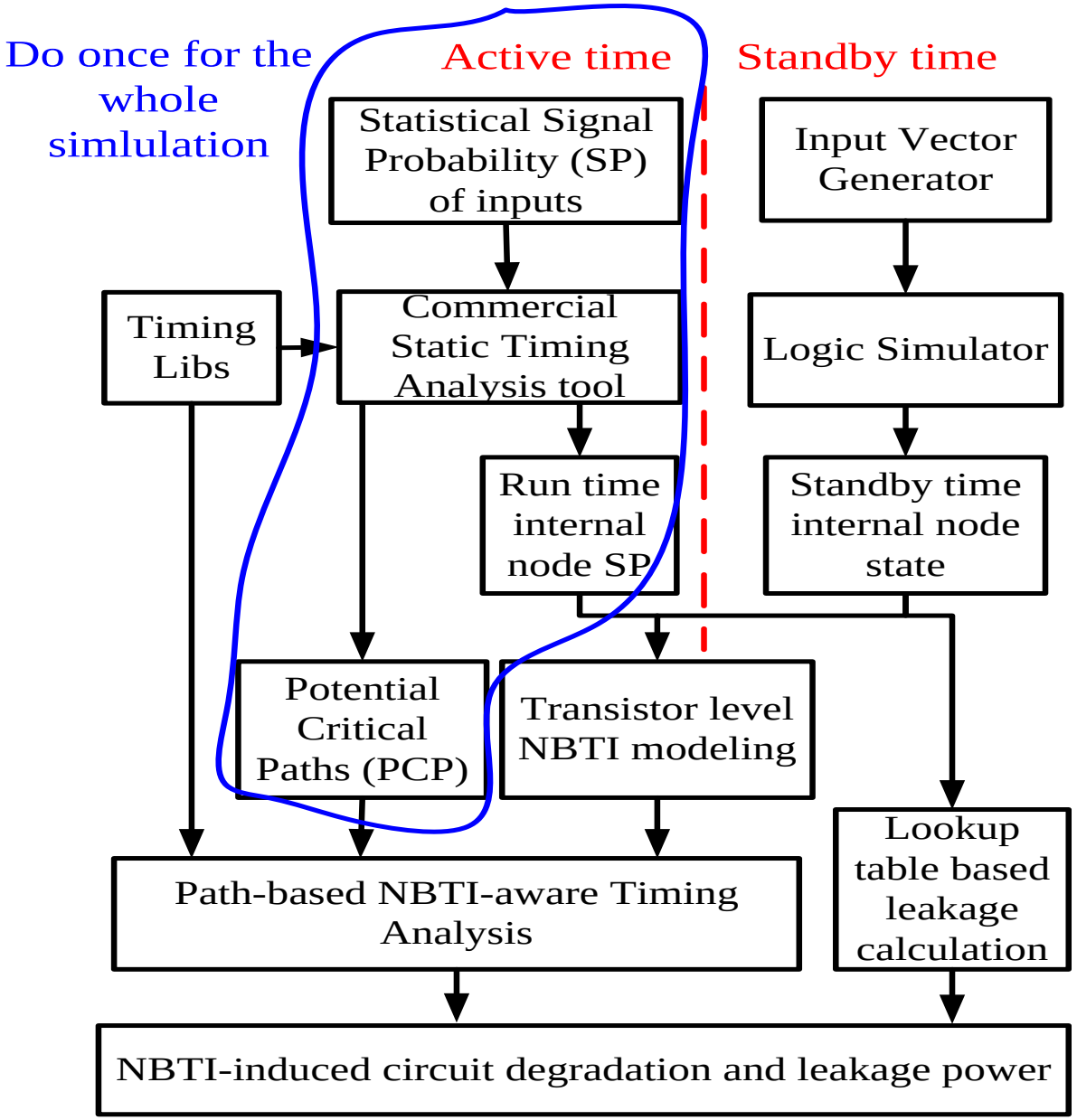
Transistor level NBTI modeling
Lookup table based leakage calculation
Path-based NBTI-aware Timing Analysis
NBTI-induced circuit degradation and leakage power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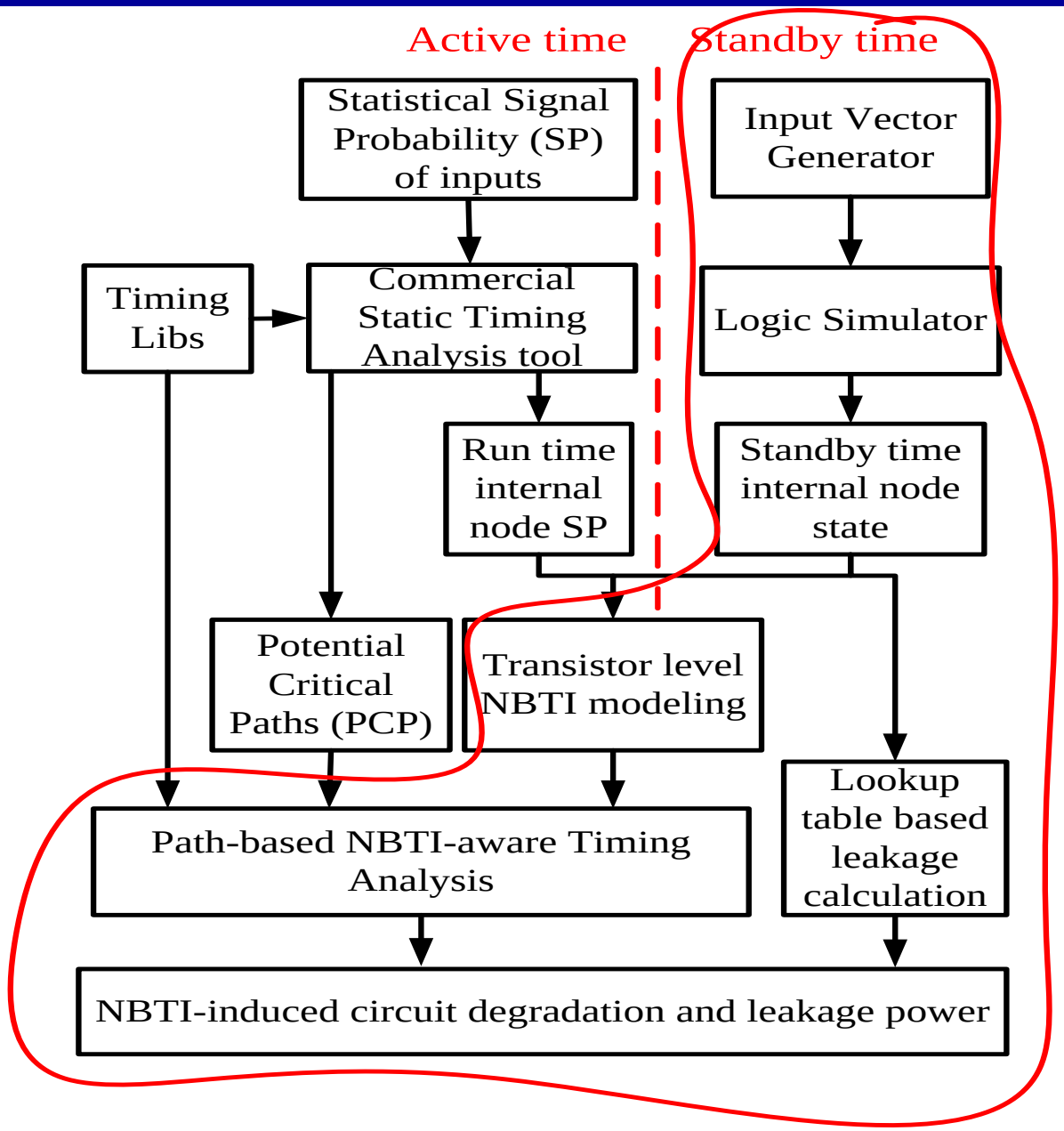
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Implementations

- C++ for most of the codes with PrimeTime
- 65nm library
- Some key technology parameters are:
  - Vdd = 1.0V ; |Vth| = 0.20V; Tox= 1.2nm
- ISCAS85 benchmark and some ALU circuits are used to evaluate our algorithms.
- Tactive and Tstandby are both set to be 378K
- Ratio of active and standby time is set to be 1:9.
- Input probabilities of all the input nodes at active time to 0.5 for simplicity.
- The circuit lifetime is set to be 10 years.
- 5% performance relaxation at time 0 is allowed

INC results (1)

- **Results of 10K random IV search in DGR**

			28.00%	**22.00 %**		**8.76%**
			28.23%	**23.30 %**		**6.16%**

TABLE II

RANDOM SEARCH RESULTS (1

Benchmark Circuits	Gate#	D_O (ns)	D_W (ns)	D_B (ns)	LK_W (mW)	LK_B (mW)
pmult4x4	122	2.522	3.154	3.004	1.17E-04	9.89E-05
c499	182	1.471	1.928	1.849	2.38E-04	2.11E-04
log16	256	1.287	1.801	1.675	2.28E-04	2.04E-04
bkung32	271	2.004	2.518	2.291	3.00E-04	2.65E-04
c432	297	3.965	4.972	4.635	2.55E-04	2.29E-04
array8x8	401	4.967	6.286	5.809	4.18E-04	3.46E-04
pmult8x8	490	4.819	6.026	5.74	4.86E-04	4.11E-04
c880	535	2.689	3.296	3.184	4.16E-04	3.76E-04
log32	640	2.138	3.231	3.047	5.67E-04	5.14E-04
c1355	942	3.089	3.733	3.67	6.60E-04	6.32E-04
c1908	977	3.763	4.548	4.355	6.93E-04	6.67E-04
c2670	1173	3.672	4.609	4.395	8.84E-04	8.49E-04
booth9x9	1206	4.195	5.057	4.883	1.14E-03	1.09E-03
log64	1536	3.862	6.259	5.967	1.36E-03	1.24E-03
c3540	1743	4.784	5.954	5.645	1.27E-03	1.20E-03
pmult16x16	1934	10.101	12.544	12.096	1.95E-03	1.67E-03
c5315	2364	4.924	6.15	5.864	1.82E-03	1.72E-03
c7552	3912	4.984	6.214	5.968	2.91E-03	2.79E-03
c6288	6656	17.94	20.886	20.379	4.69E-03	4.61E-03
pmult32x32	7570	20.921	25.784	25.247	7.65E-03	6.95E-03
average			28.00%	**22.00 %**		**8.76%**
Gate#>500			28.23%	**23.30 %**		**6.16%**

INC results (2):DGR for leakage or NBTI only

	For leakage only			For NBTI only		
	LK_{imp} (%)	Runtime (s)	a_{inc} (%)	D_{imp} (%)	Runtime (s)	a_{inc} (%)
average	**10.00%**	165.22	24.09%	**16.56%**	115.62	4.90%
Gate#>500	10.26%	269.49	30.73%	20.08%	191.47	6.52%

RESULTS OF DGR ALGORITHM FOR LEAKAGE POWER REDUCTION ONLY AND NBTI MITIGATION ONLY.

Benchmark Circuits	For leakage only			For NBTI only		
	LK_{imp} (%)	Runtime (s)	a_{inc} (%)	D_{imp} (%)	Runtime (s)	a_{inc} (%)
pmult4x4	1.037	1.938	6.81	17.23	0.43	3.546
c499	0.367	3.29	0.242	2.53	0.78	0.161
log16	16.832	5.25	22.2	17.47	1.12	1.316
bkung32	16.501	6.03	12.39	4.87	1.31	0.311
c432	23.638	7.32	25.23	6.16	1.55	5.215
array8x8	0.025	10.75	0.122	10.33	2.24	0.611
pmult8x8	0.0034	16.71	4.44	12.11	3.37	2.375
c880	18.398	19.25	41.6	19.53	4	6.199
log32	17.858	24.75	22.7	16.76	4.87	0.921
c1355	13.073	50.95	59.2	20.986	13.12	6.733
c1908	17.067	55.36	57.5	13.92	12.28	9.538
c2670	14.468	87.73	39.8	9.57	24.56	6.629
booth9x9	14.753	79.57	54.79	29.35	21.6	4.371
log64	18.442	127.6	23.2	19.43	27.1	0.932
c3540	12.496	165.2	46.9	16.35	52.5	7.783
pmult16x16	0.0003	212	4.97	17.8	44.6	2.881
c5315	0.312	315.1	39.8	22.51	109	6.96
c7552	5.678	795	5.8	16.8	409	9.961
c6288	9.049	490.2	13.9	35.19	754	13.249
pmult32x32	0.0234	830.4	0.275	22.29	825	8.318
average	**10.00%**	165.22	24.09%	**16.56%**	115.62	4.90%
Gate#>500	10.26%	269.49	30.73%	20.08%	191.47	6.52%

- **INC is more effective than IVC**
- **Larger circuits lead to better results**
- **Area increase is different for leakage and NBTI**
- **Compare to the best result of IVC**

INC results (3):DGR for leakage and NBTI

	LK_s (mW)	D_s (ns)	LK_{imp} (%)	D_{imp} (%)	a_{inc} (%)	Runtime (s)
average	5.11%	23.11%	**16.25%**	**16.51%**	14.18%	267.99
Gate#>500	3.94%	24.13%	20.75%	21.28%	16.18%	441.26

TABLE IV

RESULTS OF DGR ALGORITHM FOR SIMULTANEOUS LEAKAGE AND NBTI MITIGATION.

Benchmark Circuits	LK_s (mW)	D_s (ns)	LK_{imp} (%)	D_{imp} (%)	a_{inc} (%)	Runtime (s)
pmult4x4	1.14E-04	3.004	0.198	15.01	4.25	2.08
c499	2.11E-04	1.925	1.78	5.92	0.64	3.52
log16	2.04E-04	1.702	11.31	9.82	14.6	5.49
bkung32	2.69E-04	2.354	13.07	7.23	12.1	6.31
c432	2.38E-04	4.628	23.06	6.428	21.8	7.39
array8x8	4.06E-04	5.832	2.76	7.56	14.6	10.9
pmult8x8	4.71E-04	5.761	0.32	8.49	3.79	16.2
c880	3.80E-04	3.204	23.62	14.48	17.5	12.9
log32	5.19E-04	3.075	15.08	14.24	15.7	24.8
c1355	6.35E-04	3.686	30.63	19.571	25.4	54.5
c1908	6.71E-04	4.371	28.95	19.86	21.2	71.2
c2670	8.57E-04	4.41	22.09	12.69	18.8	97.6
booth9x9	1.09E-03	4.92	28.65	29.2	15.3	90
log64	1.26E-03	5.989	18.39	17.83	17.8	146
c3540	1.21E-03	5.707	21.05	21.25	21.9	259
pmult16x16	1.93E-03	12.14	0.26	18.15	2.61	258
c5315	1.73E-03	5.886	14.52	19.35	20.7	427
c7552	2.79E-03	6.113	21.39	27.54	11.2	1096
c6288	4.62E-03	20.73	46.98	38.53	20.7	1204
pmult32x32	7.55E-03	25.25	0.98	17.1	2.93	1567
average	5.11%	23.11%	**16.25%**	**16.51%**	14.18%	267.99
Gate#>500	3.94%	24.13%	20.75%	21.28%	16.18%	441.26

- **Compare with the results of IVC for simultaneously NBTI and leakage reduction**
- **INC is more effective than IVC**
- **Larger circuits lead to better results**

INC results (4): DCBGR for leakage and NBTI sir

	For leakage only			For NBTI only			Co-optimization			
	LK_{imp} (%)	Runtime (s)	a_{inc} (%)	D_{imp} (%)	Runtime (s)	a_{inc} (%)	LK_{imp} (%)	D_{imp} (%)	Runtime (s)	a_{inc} (%)
average	**31.73%**	1.68	11.13%	**23.65%**	1.81	3.52%	**18.93%**	**19.17%**	2.098	14.67%
Gate#>500	36.54%	2.76	13.26%	23.95%	2.99	3.53%	22.36%	22.13%	3.46	17.49%

DCBGR ALGORITHM RESULTS FOR THREE DIFFERENT OBJECT FUNCTIONS.

Benchmark Circuits	For leakage only			For NBTI only			Co-optimization			
	LK_{imp} (%)	Runtime (s)	a_{inc} (%)	D_{imp} (%)	Runtime (s)	a_{inc} (%)	LK_{imp} (%)	D_{imp} (%)	Runtime (s)	a_{inc} (%)
pmult4x4	12.71	0.047	8.94	12.12	0.015	5.11	11.76	10.4	0.031	7.23
c499	14.04	0.031	1.29	17.79	0.031	0.56	13.59	17.0	0.031	1.29
log16	39.91	0.031	0	49.61	0.047	3.04	30.34	17.47	0.047	21.05
bkung32	40.44	0.047	1.87	14.61	0.047	4.92	23.5	14.61	0.062	1.87
c432	33.41	0.047	16.41	39.88	0.047	5.06	4.98	13.82	0.047	16.64
array8x8	3.91	0.047	6.85	25.53	0.047	2.45	2.95	14.33	0.063	6.85
pmult8x8	8.28	0.078	8.36	7.57	0.078	3.61	7.7	5.97	0.078	7.4
c880	43.35	0.079	19.75	22.91	0.079	3.38	15.52	21.24	0.109	21.16
log32	40.34	0.094	0	60.23	0.11	3.42	31.11	19.87	0.141	21.05
c1355	49.81	0.172	23.8	14.24	0.172	3.73	30.26	13.22	0.234	23.8
c1908	48.24	0.172	24.38	13.88	0.203	4.13	26.11	13.88	0.266	25.84
c2670	43.74	0.297	15.96	16.76	0.328	3.4	20.19	10.44	0.422	17.39
booth9x9	40.56	0.312	8.98	9.93	0.359	2.84	35.2	5.58	0.453	8.98
log64	40.86	0.406	0	67.85	0.484	3.67	31.89	21.07	0.594	21.05
c3540	41.67	0.516	18.17	25.49	0.594	3.25	10.24	20.24	0.735	20.98
pmult16x16	5.7	0.656	7.8	11.38	0.718	2.64	5.38	9.46	0.765	7.28
c5315	39.65	1.031	14.68	9.55	1.188	3.28	15.51	9.55	1.453	17.3
c7552	47.77	2.734	18.76	48.6	3.25	4.12	25.49	19.07	4	19.89
c6288	31.26	10.75	19.15	11.04	11.672	6	28.24	10.83	14.172	19.15
pmult32x32	8.85	16.016	7.44	16.03	16.828	1.88	8.71	14.11	18.266	7.17
average	**31.73%**	1.68	11.13%	**23.65%**	1.81	3.52%	**18.93%**	**19.17%**	2.098	14.67%
Gate#>500	36.54%	2.76	13.26%	23.95%	2.99	3.53%	22.36%	22.13%	3.46	17.49%

Outline

- Background
- Internal Node Control
- Gate Replacement
- NBTI/leakage Optimization Platform
- Simulation Results
- Conclusion

Conclusion

- **INC can reduce leakage power and mitigate NBTI degradation simultaneously.**
- **INC is more effective than IVC, and INC algorithms runs more fast.**
- **For large circuits, IVC is less effective, however, INC is more effective.**
- **INC will lead to more circuit area increase (4% for NBTI only) and delay increase (5%) at time 0, which should be considered.**

Thank you

谢谢

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