Temperature-aware NBTI modeling and the impact of input vector control on performance degradation

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Abstract

[1]*As technology scales, Negative Bias Temperature Instability (NBTI), which causes temporal performance degradation in digital circuits by affecting PMOS threshold voltage, is emerging as one of the major circuit reliability concerns. In this paper, we first investigate the impact of NBTI on PMOS devices and propose a novel temporal performance degradation model for digital circuits considering the temperature difference between active and standby mode.For the first time, the impact of input vector control (to minimize standby leakage) on the NBTI is investigated. Minimum leakage vectors, which lead to minimum circuit performance degradation and remains maximum leakage reduction rate, are selected and used during the standby mode. Furthermore, the potential to save the circuit performance degradation by internal node control techniques during circuit standby mode is discussed. Our simulation results show that: 1) the active and standby time ratio and the standby mode temperature have considerable impact on the circuit performance degradation; 2) the NBTI-aware IVC technique leads to an average 3% savings of the total circuit degradation; while the potential of internal node control may lead to 10% savings of the total circuit degradation.*

1 Introduction

Circuit reliability is one of the major concerns in VLSI circuits and systems designs. Negative Bias Temperature Instability (NBTI), which has deleterious effect on the threshold voltage and the drive current of semiconductor devices, is emerging as a major reliability degradation mechenism [1].

NBTI occurs when PMOS devices in circuits are stressed under negative gate voltage (i.e., $V_{gs} = -V_{dd}$) at elevated temperature, causing a shift in threshold voltages (for example, V_{th} shifts due to NBTI can be as much as 50mV [2]), and resulting in degradation of device performance [1]. Bias temperature stress under constant voltage (DC) (i.e., static NBTI) leads to rapid device performance degradation. However, under actual AC stress condition [3, 4], when stress is periodically removed, the degradation of device parameters is partially recovered, which leads to a less severe parameter's shifts over long time compared with that under DC stress condition.

The previous work about NBTI mainly focused on the analysis of the threshold voltage degradation and the impact on the drive current of semiconductor devices [3, 5]. Recently, some analytical models that evaluate NBTI effect with multi-cycle AC stress were proposed to help designers estimate the circuit performance degradation due to NBTI [6, 7]. Based on these analytical circuit degradation models, a few researchers have investigated NBTI-aware design techniques [8, 9]. Kumar et al. [8] studied the impact of NBTI on the read stability of SRAM cells and proposed a simple bit flipping technique to recover the static noise margin of SRAM cells. Paul et al. [9] presented an NBTI-aware sizing algorithm to ensure the reliability of nano-scale circuits.

Previous analytical NBTI models for the circuit performance degradation are based on the assumption that the circuit temperature remains constant all the time; However, during circuit operations, the circuit temperature varies a lot when the circuit mode changes between active and standby state. As NBTI is temperature-dependent, and experiments indicate that at higher temperature, the degradation under stress is faster, but the recovery is slower [4]. Hence, the impact due to NBTI under a higher temperature has a large gap compared with that under a lower temperature condition. Therefore, we propose an NBTI model considering the temperature variation due to the change of circuit mode: between active and standby mode.

NBTI not only depends on the temperature, but also depends on the input states of the PMOS devices; meanwhile the leakage current of a gate also relies on the gate input states. One of the most popular leakage reduction techniques used in the circuit standby mode is the input vector control technique (IVC) [10–14]. Therefore, in this paper, we also investigate the approach of using the IVC technique to simultaneously reduce the leakage and relieve the impact of NBTI.

The IVC technique is based on the well-know transistor stack-

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ing effect: a CMOS gate's subthreshold and gate oxide leakage current varies dramatically with the input vector applied to the gate [15, 16]. Basically in an IVC technique, the minimum leakage vector (MLV) is used with the help of standby signals to reduce both subthreshold and gate oxide leakage current when the circuit is at the standby mode. When the MLV is manipulated during the circuit standby mode, the internal state of each node in the circuit is set to be 0 or 1, such that the circuit standby leakage is minimized. The continuously stress on some PMOS's in the critical paths or near critical paths may have negative impact on the circuit performance due to NBTI.

Our contribution in this paper distinguishes itself in the following aspects: (1) We study the impact of NBTI on the temporal performance degradation of combinational circuits considering temperature difference between active mode and standby mode, and propose an analytical model that takes the time ratio and temperature changes between active and standby mode into account; (2) For the first time, the impact of input vector control (to minimize standby leakage) on the NBTI is investigated. Minimum leakage vectors, which lead to minimum circuit performance degradation and remains maximum leakage reduction rate, are selected in our IVC approach. Furthermore, the potential impact of internal node control technique [13, 14] is also discussed.

The rest of the paper is organized as follows. Section 2 reviews previous NBTI models and presents our improved analytical NBTI model considering circuit active and standby mode; Section 3 presents the impact of the IVC technique considering NBTI; Section 4 shows the simulation results on the ISCAS85 benchmark circuits. Section 5 concludes the paper.

2 Temporal performance degradation analysis for digital circuits

2.1 Previous V_{th} degradation models

A shift in the transistor threshold voltage ΔV_{th} is proportional to the generation of interface traps due to NBTI, which can be expressed as [9]

$$\Delta V_{th} = (1+m)\frac{qN_{it}(t)}{C_{ox}} \tag{1}$$

where m represents equivalent V_{th} shifts due to mobility degradation for a given technology, and $N_{it}(t)$ is the interface trap density due to NBTI, which is often described by a reaction-diffusion model [2],

$$\frac{dN_{it}}{dt} = k_f(N_0 - N_{it}) - k_r N_{it} C_H(0,t) \tag{2}$$

$$\frac{dN_{it}}{dt} = -D_H \frac{\partial C_H}{\partial x}\bigg|_{x=0} \tag{3}$$

where the mobile diffusing species are assumed to be neutral H atoms, and N_0 is the concentration of initial interface defects. The parameters k_f and k_r are constant dissociation rate and self-annealing rate, respectively. When the device is in recovery phase, k_f becomes zero, and k_r is unchanged. The parameter C_H is the concentration of H atoms, and D_H is the corresponding diffusion coefficient.

The diffusion of H D_H, which has great impact on N_{it}, follows the equation [2]:

$$\frac{\partial C_H}{\partial t} = D_H \frac{\partial^2 C_H}{\partial x^2} \tag{4}$$

With assumption of quasi-equilibrium and an infinite thick oxide (i.e. t_{ox} is more than diffusion length $\sqrt{4D_H t}$), a solution of Eq. (2)-(4) is given by [2]:

$$N_{it}(t) = 1.16(\frac{k_f N_0}{k_r})^{1/2}(D_H t)^{1/4} = At^{1/4} \tag{5}$$

Eq.(5) describes the NBTI impact under DC stress condition. When the stress is removed after a stress time of t_{stress}, an analytical form for recovery process is given by [7]

$$N_{it}(t) = N_{it}^0(1+\sqrt{t/t_{stress}})^{-1} \tag{6}$$

where t is the recovery time and N_{it}^0 is the interface density at the beginning of recovery.

2.2 Our NBTI Model for V_{th} degradation

The above models have described both the stress and recovery phases of the NBTI degradation; however, in order to estimate the performance degradation of a circuit, the NBTI model should handle multiple cycles of stress and recovery phases. Therefore, a multi-cycle analytical model should be used.

An analytical NBTI model was proposed in [7] to handle multi-cycle AC stress condition; and the creation of interface traps after n cycles of AC stress can be evaluated by a recursion formula. The generation of interface traps assuming DC stress over the first period (i.e. a stress of time τ) is denoted as $N_{it}^0 = A\tau^{1/4}$; so after n cycles of AC stress, the interface traps can be expressed as [7]:

$$N_{it}[(n+1)\tau] = \frac{\beta}{1+\beta} + \frac{N_{it}^0}{1+\beta}\left[c + \left(\frac{N_{it}(n\tau)}{N_{it}^0}\right)^4\right]^{1/4} \tag{7}$$

and

$$N_{it}(\tau) = \frac{c^{1/4}}{1+\beta} N_{it}^0 \tag{8}$$

where τ is the period time, c is duty cycle of stress phase, and $\beta = \sqrt{\frac{1-c}{2}}$.

Considering a large enough cycle number n, we further simplify the recursion based on Eq.(7)(8) [7],

$$S_1 = \frac{c^{1/4}}{1+\beta} \tag{9}$$

$$S_{n+1} = S_n + \frac{c}{4(1+\beta)S_n^3} \tag{10}$$

and

$$N_{it}(n\tau) = S_n N_{it}^0 = S_n \cdot A\tau^{1/4} \tag{11}$$

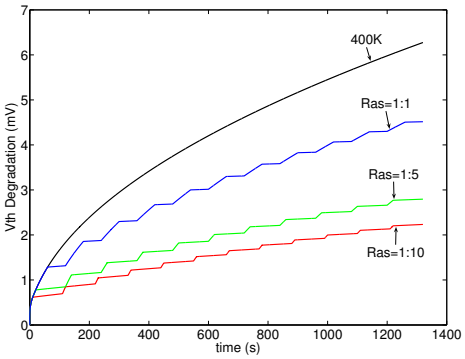

Figure 1. V_{th} degradation with different active and standby time ratio (Ras) under continuously stress

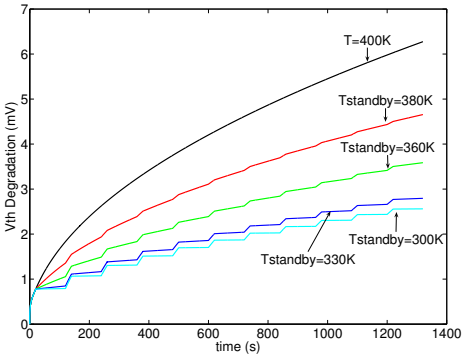

Figure 2. V_{th} degradation with different $T_{standby}$ under continuously stress

From Eq. (1), the shifts of threshold voltage can be expressed as

$$\begin{aligned}\Delta V_{th}(n\tau) &= (1+m)\frac{q}{C_{ox}} \cdot S_n \cdot A\tau^{1/4} \\ &= K_V S_n \tau^{1/4}\end{aligned} \tag{12}$$

where K_V is a constant related with E_{ox} and temperature, S_n is controlled by duty cycle.

During circuit operations, the circuit mode changes between active and standby states, so that the circuit temperature changes periodically. Previous NTBI models only consider the situation that the temperature is a constant (which is around 400K). We assume the circuit temperature during the active mode and standby mode are T_{active} and $T_{standby}$, respectively. The circuit operation temperature changes between T_{active} and $T_{standby}$ frequently, hence the impact on V_{th} due to NBTI should be different from the case under a constant high operation temperature condition.

The temperature variation has a significant impact on the diffusion coefficient of H atom D_H in Eq.(5). If a triangle diffusion profile [2] is used to model D_H, the effect of H atom diffusion under $T_{standby}$ lasting for a stress time of $t_{standby}$, equals to the effect under T_{active} for a stress time of $t'_{standby}$, where $t'_{standby} = D_{standby} \times t/D_{active}$ ($D_{standby}$ and D_{active} denote diffusion coefficients under standby and active mode, respectively). Therefore, the equivalent stress time t^{eq}_{stress} for each cycle can be expressed as,

$$t^{eq}_{stress} = t_{active} + t_{standby}\frac{D_{standby}}{D_{active}} \tag{13}$$

The equivalent recovery time $t^{eq}_{recovery}$ can be considered similarly.

The equivalent duty cycle c^{eq} and period time τ^{eq} can be derived as

$$c^{eq} = \frac{t^{eq}_{stress}}{t^{eq}_{stress} + t^{eq}_{recovery}} \tag{14}$$

$$\tau^{eq} = t^{eq}_{stress} + t^{eq}_{recovery} \tag{15}$$

With the equivalent duty cycle c^{eq} and period time τ^{eq}, the ΔV_{th} considering the time and temperature changes between active and standby mode can be evaluated using Eq. (9)-(12).

Fig. 1 shows the impact on ΔV_{th} with different active and standby time ratios (Ras). The temperature of highest line is $T_{standby} = T_{active} = 400K$; the temperature of others is $T_{standby} = 330K$. Fig. 2 shows the impact on ΔV_{th} with $T_{standby}$. The active and standby time ratio is set to be 1:5. These two figures show that the active and standby time ratio and the standby mode temperature have great impact on the V_{th} degradation due to NBTI.

2.3 Gate and circuit delay degradation

In this paper, a combinational circuit is modeled by a directed acyclic graph (DAG) $G = (V, E)$. A vertex $v \in V$ represents a CMOS gate from the given library, while an edge $(i, j) \in E$, $i, j \in V$ represents a connection from vertex i to vertex j.

The delay of a gate v can be approximately expressed as [9],

$$\begin{aligned}d(v) &= \frac{C_L V_{dd}}{I_d} = \frac{K}{(V_g - V_{th})^\alpha} \\ K &= \frac{C_L V_{dd}}{\mu C_{ox} W_{eff}/L_{eff}}\end{aligned} \tag{16}$$

where C_L is the load capacitance, V_{dd} is the supply voltage; V_g and V_{th} are the gate voltage and the threshold voltage of a transistor, respectively; α is the velocity saturation index, whose value ranges from 1 to 2; μ is the mobility, C_{ox} is the oxide capacitance, and L_{eff} and W_{eff} are the channel length and the transistor width respectively.

Hence, the delay degradation $\Delta d(v)$ for gate v can be derived as:

$$\begin{aligned}\Delta d(v) &= \frac{K}{(V_g - V_{th} - \Delta V_{th})^\alpha} - \frac{K}{(V_g - V_{th})^\alpha} \\ &= \left((1 - \frac{\Delta V_{th}}{V_g - V_{th}})^{-\alpha} - 1\right) d(v)\end{aligned} \tag{17}$$

We use Taylor series expansion on the right side of Eq.(17), neglect the higher order terms, such that,

$$\Delta d(v) = \frac{\alpha \Delta V_{th}}{V_g - V_{th0}} \times d(v) \tag{18}$$

where V_{th0} is the original transistor threshold voltage and $d(v)$ is the original delay of gate v. There might be several ΔV_{th} of different PMOS's in one gate. In such cases, we just select the largest one to calculate the gate delay degradation, which is the worst case delay degradation. The shift in the transistor threshold voltage, ΔV_{th}, can be derived using Eq. (12). The signal probability for each edge in the circuit can be derived statistically by simulating a large number of input vectors.

Given a time interval, we can have the corresponding gate delay degradation from Eq.(18). A static timing analysis tool [17] is used to compute the max delay of the circuit with all the gates' temporal degradation information.

3 Impact of Input Vector Control(IVC) technique on performance degradation

Since NBTI and leakage current both depend on internal states of the circuits (i.e., the input states of gates), in this section, we study the impact of the IVC technique on circuit degradations due to NBTI. The potential to save the circuit performance degradation by internal node control techniques [13, 14] during circuit standby mode is discussed.

3.1 Our IVC technique

A leakage lookup table is created by simulating all the gates in the standard cell library under all possible input patterns. Thus the leakage current $I_{leakage}(v)$ can be expressed as:

$$I_{leakage}(v) = \sum_{IN} I_l(v, IN) \times Prob(v, IN) \tag{19}$$

where $I_l(v, IN)$ and $Prob(v, IN)$ are the leakage current and the probability of gate v under input pattern IN.

Finding MLV is proved to be NP-complete; both exact and heuristic approaches have been proposed to search for the MLV [10–12]. In this paper, we first find a set of MLV's using a simple probability based method; then investigate the impacts of different MLV's on the performance degradation due to NBTI; and finally MLV's that simultaneously achieve the minimum circuit performance degradation and the maximum leakage reduction rate are selected.

The pseudo-code for our probability-based algorithm to select an MLV set is shown in Fig.3. The probability based algorithm begins by generating N random vectors; and the leakage current of each vector in the MLV set is within a given range of the minimum leakage current in the set. Next, for each primary input, the probability is calculated by the number of 1s out of the total number of vectors. New vectors are generated using the calculated probabilities. The leakage current of each new input vectors are calculated and the MLV set is updated. The probabilities for all primary inputs will converge to either 0 or 1, and it means that there is no probability of generating other vectors. So this is the convergence point of circuit leakage current and the algorithm is halted.

Using a circuit logic simulator, the internal state of each edge can be derived for each MLV. The $\Delta d(v)$ for a given period of time of each gate v is evaluated referring to Eq.(18) in Section 2.3. Based on these information, the static timing analysis tool is used to get the overall circuit delay degradation for each MLV in the MLV set. We choose the MLV with the minimum circuit delay degradation to be the one used in the circuit standby mode.

```
Probability based MLV selection algorithm
  0 Generate N random input vectors (IV)
  1 Select an MLV set S within a leakage range
  2 Compute the probability of each primary input
  3 Use the probability to generate new IVs
  4 Calculate circuit leakage using new IVs
  5 If the circuit leakage current is converged
       Output the MLV set
  6 Else
       Jump back to step 1
```

Figure 3. A probability-based algorithm to select an MLV set

3.2 Potential of internal node control

The timing and area overhead of the IVC technique, which is caused by the flip-flop at the primary inputs of the circuits, can be neglected for a large digital circuit design; however, for large circuits, the internal states can not be well controlled by the primary input vectors, thus the leakage variance due to different input combinations is not very large, and the MLV's may not result in a significant leakage reduction. Because of the same reason, different MLV's may not result in large difference of impact on circuit degradation.

Lin et al. [13] pointed out that if the internal node deep in the circuit can be manipulated, greater leakage current reduction can be achieved. If the internal nodes can be controlled to reduce the leakage during the circuit standby mode, they can be also controlled to relieve the NBTI impact. Assuming all the PMOS's in the critical paths and near-critical paths are driven by the supply rail during the circuit standby mode (i.e., all PMOS devices are driven by '1'), the circuit performance degradation will be minimized.

4 Simulation results

In this section, we present the experimental results on ISCAS85 benchmarks. All ISCAS85 benchmark circuit netlists are synthesized using a commercial synthesis tool and mapped to a 90nm standard cell library. A leakage current lookup table of all the standard cells is generated using HSPICE. The $90nm$ standard cell library is constructed using the PTM 90nm bulk CMOS model [18].

Table 1. ΔV_{th} under different active and standby mode ratio (mv)

Ratio	9 : 1	7 : 1	5 : 1	3 : 1	1 : 1	1 : 3	1 : 5	1 : 7	1 : 9
$T_{standby} = 400K$	22.0916	22.2015	22.3824	22.7374	23.7743	24.8526	25.2592	25.4846	25.6317
$T_{standby} = 330K$	21.2571	21.1569	20.9857	20.6258	19.3643	17.6461	16.8849	16.4467	16.1612

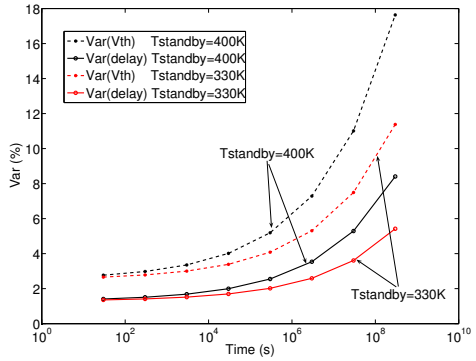

Figure 4. Performance degradation of C432

$V_{DD} = 1.0V$, $|V_{th}| = 220mV$ are set for all the gates in the circuit. The original gate delays are also extracted using the commercial synthesis tool. The switching activity of each individual gate and the internal nodes' states for each MLV are evaluated using a self-developed logic simulator. MATLAB NBTI model and a static timing analysis (STA) tool [17] are used to calculate the circuit performance degradation. The probability based MLV selection algorithm is implemented using C++. The simulations are conducted on a 1.83G HZ cpu, 1.5G memory computer.

4.1 Degradation analysis

The V_{th} degradation under continuously stress with different active and standby time ratios is shown in Table 1. The total time is set to $3 \times 10^8 s$ and the signal probability during the active mode is set to 0.5. When $T_{standby} = T_{active} = 400K$, the ΔV_{th} is increasing with a decreasing active and standby time ratio, since the total time under stress condition is increased. However, the ΔV_{th} is decreasing when $T_{standby} = 330K$ with a decreasing active and standby time ratio, since the total time under lower temperature is increased. The largest gap between the ΔV_{th} is about $9.4mv$ when the active and standby time ratio is 1:9.

In the circuit degradation analysis, we set all the internal nodes' states to 0 during the standby mode, to investigate the worst case circuit degradation. Fig. 4 shows the performance degradation of ISCAS85 C432 benchmark with time under different standby mode temperature. The circuit degradation is much less than the V_{th} degradation under a same standby mode temperature. And the standby mode temperature difference leads to considerable circuit delay difference.

Table 2. NBTI-aware IVC technique

Circuits	Gate number	Nominal delay(ns)	$\Delta delay$ (%)	MLV difference (%)
c432	169	2.69	5.06	0.24
c499	204	1.99	5.62	0.17
c880	383	2.29	5.66	0.22
c1355	548	2.39	5.38	0.17
c1908	911	2.46	5.19	0.12
c2670	1279	2.99	5.58	0.20
c3540	1699	3.48	5.39	0.13
c5315	2329	2.94	5.28	0.20
c6288	2447	8.54	6.20	0.09
c7552	3566	2.30	5.27	0.10

4.2 Impact of IVC technique

We use probability based MLV selection method to select a set of MLV, in which the leakage current difference of any MLVs are within 4% of the original circuit leakage current. The impact of these MLVs are investigated to find an MLV with minimum circuit performance degradation.

In Table 2, we show that the minimized $\Delta delay$ using our IVC technique is about on average 5.4% of the circuit delay; while the performance impact difference of different MLV is about 0.15% of the original circuit delay and 3% of the $\Delta delay$. Here, the active and standby time ratio is set to 1:5; the $T_{standby} = 330K$.

Because the standby mode temperature is much lower compared with the active mode temperature, the impact of MLV selection technique is not very impressive, but it will be larger with a higher standby mode temperature. The internal node states deep in a large circuits can not be controlled effectively by the primary inputs. Therefore, for larger circuits, the MLV impact on both leakage current and NBTI induced circuit performance degradation is smaller.

4.3 Potential of internal node control

We further evaluate the difference of the maximized performance degradation (all the PMOS devices are driven by '0') and the minimized performance degradation (all the internal nodes are driven by '1'). This circuit delay difference is defined as the potential of the internal node control technique. In Table 3, we show the delay degradation of ISCAS85 benchmarks and the potential of internal node control under different standby mode temperature. The active and standby ratio is set to 1:5. The max $\Delta delay$, which is derived by setting all the internal nodes to 0, is around 8.6% of the original circuit delay when $T_{standby} = 330K$; and is around 5.8%

Table 3. Delay degradation of ISCAS85 benchmarks under NBTI and potential of internal node control

ISCAS85 Benchmark Circuits	$T_{standby} = 400K$		$T_{standby} = 330K$	
	Max $\Delta delay(\%)$	Potential (%)	Max $\Delta delay(\%)$	Potential (%)
c432	8.41	3.41	5.42	0.565
c499	8.57	3.16	5.81	0.550
c880	8.65	3.16	5.92	0.602
c1355	8.46	3.27	5.60	0.544
c1908	8.44	3.38	5.53	0.602
c2670	8.60	3.15	5.86	0.562
c3540	8.48	3.22	5.66	0.524
c5315	8.46	3.24	5.56	0.499
c6288	8.90	3.06	6.44	0.748
c7552	8.42	3.28	5.51	0.507

of the original circuit delay when $T_{standby} = 330K$. The potential of the internal node control technique is about 10% of the max $\Delta delay$ when $T_{standby} = 330K$. But when $T_{standby} = 400K$, the potential of the internal node control technique reaches about 39% of the maximum circuit delay degradation. Furthermore, the potential will be larger with a larger active and standby time ratio, because the total time that spends in the standby mode will be increased.

Not all the internal nodes on the critical or near critical paths can be pratically set to 1 or 0; so this potential can be a reference of the largest performance saving by applying internal node control techniques.

5 Conclusion and future works

In this paper, we propose an improved temporal NBTI-induced performance degradation model for digital circuits . The standby mode temperature and the active and standby time ratio, which have significant impact on circuit performance degradation due to NBTI, are considered in our model for the first time. We study the impact of IVC technique (which leads to maximum leakage reduction during circuit standby mode) on circuit performance degradation due to NBTI. Although the impact difference of different MLVs on the circuit performance is not very impressive, we analyze the potential of saving the circuit performance degradation by internal node control techniques, and find out the potential is about 10% of the max $\Delta delay$ when $T_{standby} = 330K$. Furthermore, when $T_{standby} = 400K$, the potential of the internal node control technique reaches about 39% of the maximum circuit delay degradation.

How to perform internal node control to reduce the leakage current and relieve the impact of NBTI under a certain performance requirement is an interesting problem, which will be one of our future works.

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