All Spin Artificial Neural Networks Based on Compound Spintronic Synapse and Neuron

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***Abstract*—Artificial synaptic devices implemented by emerging post-CMOS non-volatile memory technologies such as Resistive RAM (RRAM) have made great progress recently. However, it is still a big challenge to fabricate stable and controllable multilevel RRAM. Benefitting from the control of electron spin instead of electron charge, spintronic devices, e.g., magnetic tunnel junction (MTJ) as a binary device, have been explored for neuromorphic computing with low power dissipation. In this paper, a compound spintronic device consisting of multiple vertically stacked MTJs is proposed to jointly behave as a synaptic device, termed as compound spintronic synapse (CSS). Based on our theoretical and experimental work, it has been demonstrated that the proposed compound spintronic device can achieve designable and stable multiple resistance states by interfacial and materials engineering of its components. Additionally, a compound spintronic neuron (CSN) circuit based on the proposed compound spintronic device is presented, enabling a multi-step transfer function. Then, an All Spin Artificial Neural Network (ASANN) is constructed with the CSS and CSN circuit. By conducting system-level simulations on the MNIST database for handwritten digital recognition, the performance of such ASANN has been investigated. Moreover, the impact of the resolution of both the CSS and CSN and device variation on the system performance are discussed in this work.**

***Index Terms*—All Spin Artificial Neural Network (ASANN), artificial synaptic device, compound spintronic device, magnetic tunnel junction (MTJ), post-CMOS non-volatile memory (NVM) technologies, resistive RAM (RRAM).**

I. Introduction

NEUROMORPHIC computing based on Artificial Neural Networks (ANNs) has advantages over Von-Neumann architecture based digital computing paradigm in terms of its massive parallelism, adaptivity to the varying and complex input information, energy-efficiency and inherent tolerance to fault and variation [1], [2]. In the ANNs, neurons and synapses are the two basic computing elements. The neural computation is performed by weighted summation of input neuron signals subjecting to transfer function of output neurons. For example, if the input neuron signals are represented by $\{I_i\}$ and the corresponding synaptic weights are represented by $\{w_i\}$, then the output neuron signals can be represented by $y = f(\sum w_i \cdot I_i)$ [3], where f represents the transfer function of the output neuron, which could be a step, linear or sigmoid function. The synapse contributes to the computation by modulating its weight according to the output signals of its pre- and post-neuron [4]. However, custom analog/digital CMOS implementations of the neurons [5] and synapses [6] have been proved to be extremely area and power inefficiency, since they cannot provide a direct mapping to the thresholding operation and tunable weights involved in neuromorphic computing [7].

In human brain, there are 10^{14} synapses and 10^{10} neurons. It is clear that the synapses outnumber the neurons by several orders of magnitude [4]. Thus, research work has been focused on how to mimic the biological synapse functionality using the emerging post-CMOS non-volatile memory (NVM) technologies such as resistive RAM (RRAM) and spin transfer torque magnetic RAM (STT-MRAM) with low power dissipation and high density in the form of crossbar [8]–[26]. Although it has made great progress recently, there still exists great difficulties to fabricate controllable and stable multilevel RRAM. While in the case of using STT-MRAM as synapses, the situation and difficulty are different. In order to acquire learning ability, its intrinsic STT switching stochasticity is introduced since each magnetic tunnel junction (MTJ), the basic storage cell of STT-MRAM, is a binary device [8]. However, this leads to a worse learning accuracy and redundancy is required to achieve learning accuracy as high as that achieved by the analog-like synapse with RRAM.

In our previous study [27], we have shown that a compound spintronic device (CSD) that consists of multiple vertically stacked MTJs can achieve multiple resistance states by manipulating the critical switching current and resistance area

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product of its components. Different from the RRAM, the multilevel CSD is highly controllable. Even the separation of any two adjacent resistance levels can be finely adjusted to fulfill the requirement of the whole neuromorphic computing system. In our novel approach, the critical switching current and resistance area product of the MTJ can be adjusted by the interfacial perpendicular magnetic anisotropy (PMA) with interfacial and material engineering. In this paper, a compound spintronic synapse (CSS) is proposed by using the multilevel CSD. Crossbar structure of the proposed CSS is employed for high density. On the other hand, a limitation in the existing work [28] is that the spintronic neuron could only emulate the step transfer function in the ANNs (corresponding to the switching between its two state states by a resultant synaptic current), whereas the non-step like (e.g., linear and sigmoid) transfer function can be more attractive for complex pattern recognition tasks since more information can be encoded in the neuron activity. In order to address this problem, a compound spintronic neuron (CSN) circuit based on the multilevel CSD is also proposed, which can implement a multi-step transfer function. Additionally, we construct an all spin artificial neural network (ASANN) by combining the proposed CSS and CSN circuit together. Furthermore, a study case is made on MNIST database for handwritten digital recognition.

This article is organized as follows. Section II presents the design methodology and fabrication process for multilevel compound spintronic device (CSD). In Section III, the compound spintronic synapse (CSS) and neuron (CSN) circuit are proposed. Circuit-level simulations of the proposed CSS and CSN circuit are performed with considerations of device variation. Then, an all spin artificial neural network (ASANN) consisting of the proposed CSS and CSN circuit is illustrated and the performance of such ASANN with off-line training is investigated by performing system-level simulations in Section IV. Section V concludes this paper and then discusses future research directions.

II. Design Methodology for Proposed Multilevel Compound Spintronic Device

A. *Fundamentals of STT-MTJ*

By exploiting the electron spin property instead of electron charge, spintronic devices can offer numerous novel features, such non-volatility, low power, etc. Most spintronic devices are based on magnetic tunnel junction (MTJ) structure as shown in Fig. 1(a). A MTJ is mainly composed of one one ultra-thin tunneling barrier (TB) layer (e.g., MgO) sandwiched by two ultra-thin ferromagnetic (FM) layers (e.g., CoFeB). In order to store one bit binary information, these two FM layers are set to be asymmetric. It means that the magnetization orientation of one FM layer is fixed in one direction, called pinned layer (PL), while that of the other FM layer is reversible, named free layer (FL). For the TB layer, it functions as a spin filter. If the magnetization orientation of these two FM layers is parallel, the current flow depends on the tunneling electron exchange between majority spin polarization of both the PL and the FL. Due to the large Density of State (DOS) of majority spin, the resistance of the MTJ in this configuration is small. On the other hand, the current flow depends on the tunneling electron exchange between the majority and minority spin polarization of both the PL and the FL. Due to the small DOS of minority spin, the resistance of the MTJ in this configuration is large. Generally, the resistance ratio of the MTJ in the parallel and anti-parallel configuration is characterized by the tunneling magnetoresistance (TMR), which is defined as

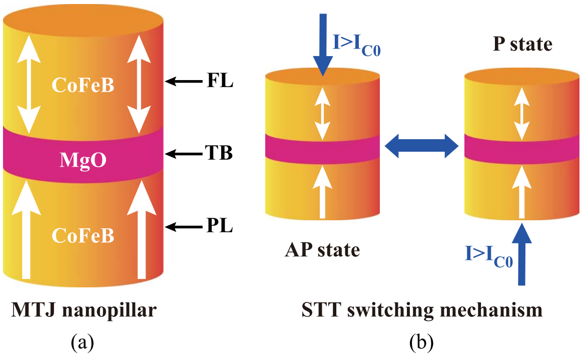


Fig. 1. (a) Vertical structure schematic of a MTJ nanopillar with perpendicular magnetization anisotropy composed of CoFeB/MgO/CoFeB thin films. (b) Spin transfer torque (STT) switching mechanism: the resistance state of the MTJ nanopillar can be reversed by a bidirectional current. Here, FL, TB and PL are short for free layer, tunnel barrier and pinned layer, respectively.

$$\mathrm{TMR} = \frac{R_{\mathrm{AP}} - R_P}{R_P} \tag{1}$$

where R_{AP} is the electrical resistance in the anti-parallel (AP) state, whereas R_P is the resistance in the parallel (P) state.

The spin transfer torque (STT) effect is an effect in which the magnetization orientation of the FL in one MTJ can be switched by applying a spin-polarized current, and it is an inverse effect of spin polarization. As shown in Fig. 1(b), an unpolarized charge current (consisting of 50% spin-up and 50% spin-down electrons) passes through the PL to the FL and becomes a spin-polarized current. When the spin-polarized current arrives into the FL, angular momentum carried by the spin-polarized current can be transferred to this layer, changing its orientation to be parallel with the PL. If an unpolarized electric current passes through the FL to the PL. The electrons with spin direction parallel to majority spin in the PL can tunnel into the PL, and those electrons with the other spin direction is left in the FL. Angular momentum carried by these electrons left in the FL is transferred to this layer, changing its orientation to be anti-parallel with the PL. Since the STT effect is purely an electrical effect without magnetic field, it is critical for STT-MRAM to achieve high speed, low power and scalability.

The explosive growth of computation power needed by the modern information society demands the memory chips with high capacity and low power. In order to meet this requirement, the dimension of the MTJ should be scaled down to below 40 nm. However, the critical switching current of the MTJ with in-plane magnetic anisotropy (i-MTJ) cannot be continuously reduced with shrinking device size. Recent material progress showed that the MTJ with perpendicular magnetic anisotropy (p-MTJ) as seen in Fig. 1(a) can offer lower critical switching current and higher switching speed in comparison with the

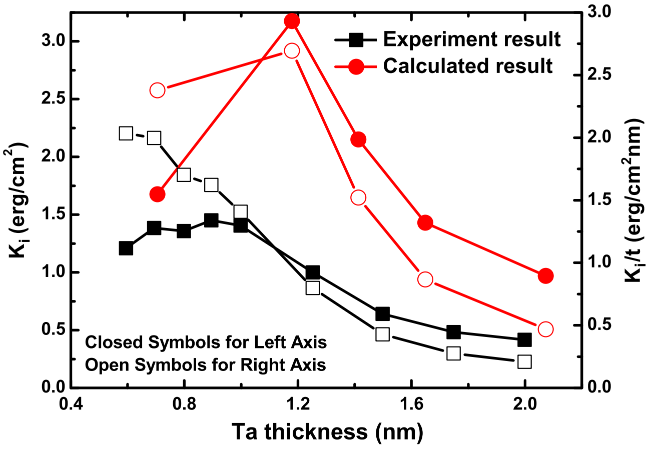


Fig. 2. The calculated K_i and K_i/t from first-principle calculations as well as experimental results are shown. It can be seen that the theoretical calculations give the same trends as experimental measurements.

i-MTJ. The critical switching current can be expressed as for the p-MTJ [29]

$$I_{c0} = \alpha \frac{\gamma e}{\mu_B g} (\mu_0 M_s) H_k V \tag{2}$$

where α is the Gilbert damping factor, γ is the gyromagnetic ratio, e is the electron charge, μ_B is the Bohr magneton, g is a parameter corresponding to the spin polarization and the magnetization orientation angel between the FL and the PL, μ_0 is the permeability in the free space, M_s is the saturation magnetization, H_k is the perpendicular magnetic anisotropy (PMA) field and V is the volume of the FL. According to this equation, it is implied that the critical switching current can be manipulated if the PMA field H_k can be tuned.

B. Interface Engineering for PMA Field

The relationship between the PMA field H_k and the effective magnetic anisotropy constant K_{eff} is written as [27]

$$K_{\text{eff}} = \frac{M_s H_k}{2}. \tag{3}$$

For ultra-thin film structure, both bulk and interface effect contribute to the effective magnetic anisotropy constant K_{eff}. Thus K_{eff} can be described by [27]

$$K_{\text{eff}} = K_b + K_d + K_i/t \tag{4}$$

where K_b is bulk anisotropy, K_d is demagnetization field and can be termed as $K_d = -2\pi M_s^2$, and K_i is interfacial PMA and t is the thickness of magnetic layer.

According to our recent theoretical work [30], it has been revealed that the interfacial PMA in the CoFeB/MgO/CoFeB ultra-thin film structure comes from both the MgO/CoFe and CoFe/capping layer interfaces. Furthermore, we have shown that the contribution of interfacial PMA from the MgO/CoFe and CoFe/capping layer interfaces are additive, which can be tuned separately. In Fig. 2, the calculated K_i and K_i/t from first-principle calculations as well as experimental results are shown. As seen, the theoretical calculations exhibit the same trends with experimental measurements. The interfacial PMA changes significantly as the thickness of the Ta film varies. The maximum value of interfacial PMA is at the Ta thickness of ~1–1.2 nm.

Further, the interfacial PMA originated from other capping layer materials have been calculated as shown in Table I [30]. The second last column shows the sum from the magnetic anisotropy energy (MAE) at the interface of the MgO/CoFe and CoFe/X, where the X includes Ru, Ta and Hf. It can be observed that the interfacial PMA can be tuned by different capping layer materials as well as different capping layer thickness. By carefully designing the capping layer materials and their thickness, we can achieve critical switching current with several times of changing range.

C. Proposed Compound Spintronic Device

To achieve multiple resistance states, we proposed a compound spintronic device, which consists of multiple vertically stacked MTJs as shown in Fig. 3(a). The critical switching current and resistance area product (RA) of each MTJ can be modulated separately. The former can be tuned by choosing different capping layers materials and their thickness, while the latter by varying the MgO thickness and other fabrication process parameters. It is apparent that by using our proposed design methodology, the proposed compound spintronic device can exhibit multiple more designable and controllable resistance states in comparison with the RRAM device.

Furthermore, we are also trying to fabricate the proposed device, and Fig. 3(b) shows the TEM image of the fabricated compound spintronic device with two vertically stacked MTJs. The 14 layer stack is Ta(5)/Ru(10)/Ta(5)/CoFeB(1)/MgO(0.85)/CoFeB(1.4)/Ta(5)/Ru(5)/Ta(5)/CoFeB(1.2)/MgO(1)/CoFeB(1.6)/Ta(5)/Ru(5), where the numbers indicate the layer thickness in nanometer. These two vertically stacked MTJs with different MgO and capping layer thickness are implemented. The critical switching current and RA of these two MTJs are different for the capping layer and MgO tunneling barrier are intendedly deposited with different thickness. Since we are working on the optimization of the multi-step etching process of these complex layer stack to avoid deteriorating of the MTJ profile and performance, we have not had a chance to perform experimental measurements on the proposed compound spintronic device.

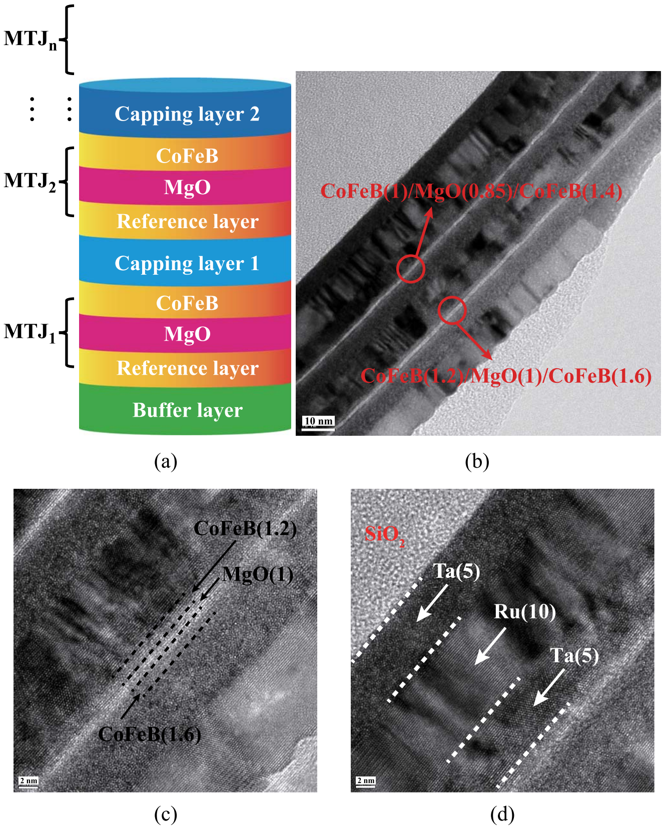
However, the performance of the proposed compound spintronic device with two vertically stacked MTJs was evaluated with a physics-based STT-MTJ compact model [31], which was programmed with the Verilog-A language and performed on the Cadence Platform. In the model, M_s was set to be 1150 emu/cm^3 according to the experimental results published in [32] and [33]. H_k of each MTJ is calculated from simulation results and chosen to be 3057 and 1520 Oe for the Ta film with thickness of ~1.35 and 1.65 nm, respectively. The TMR is set to be 200% for both the MTJs. In order to achieve maximum separations between each resistance state for better system level performance, the relation between RA of these two MTJs is written as

$$\text{RA}_2 = 2 \times \text{RA}_1 \tag{5}$$

where $\text{RA}_1 = 5\ \Omega \cdot \mu\text{m}^2$.

TABLE I
CALCULATED MAE VALUES (erg/cm^2) FOR DIFFERENT STRUCTURES

X	CoFe surface	MgO/CoFe interface	CoFe/X interface	Sum of MAE in two interfaces	MgO/CoFe/X structure
Ru	0.41	0.57	0.52	1.09	0.98
Ta	0.41	0.57	1.13	1.70	1.77
Hf	0.41	0.57	1.65	2.22	2.28



(a) (b)

(c) (d)

Fig. 3. (a) Schematic of the proposed compound spintronic device. The capping layer materials/thickness and MgO tunneling barrier thickness can be manipulated separately to obtain desired multilevel states. In ideal case, N vertically stacked MTJs can exhibit 2^N states. (b). TEM picture of the fabricated two vertically stacked MTJs with capping layers. (c) Zoom in of the CoFeB/MgO/CoFeB structure (d) Zoom in of the Ta/Ru/Ta capping layers.

By performing the DC simulation with the above parameters, Fig. 4 shows the $R - I$ loop of the proposed compound spintronic device (with two MTJs) corresponding to fabricated devices in Fig. 3(b). In the simulation, the size of both the MTJs is set to be 40 nm. It can be observed that by properly adjusting the capping layer and MgO tunneling barrier thickness, four distinct states can be obtained with well separated critical switching current and relevant resistance. The critical switching currents of these two MTJs are $\sim$50 μA and $\sim$100 μA, respectively. The simulation clearly verifies that the proposed compound spintronic device is designable and stable in comparison with almost uncontrollable multilevel RRAM. Moreover, it can be inferred that by vertically stacking more MTJs, more resistance states can be obtained. In the ideal case, the 2^N resistance states can be achieved by stacking N MTJs.

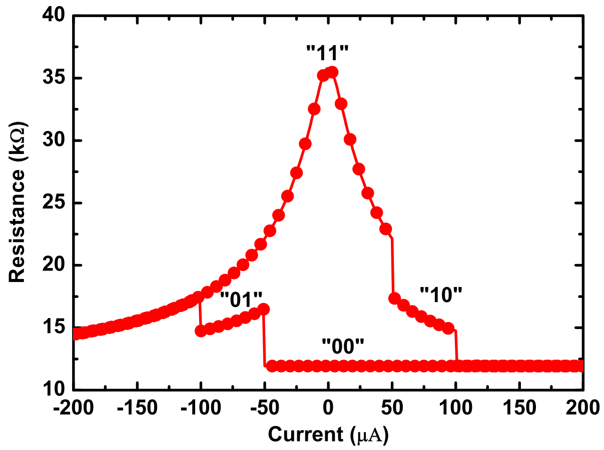


Fig. 4. Electrical characterazation of $R - I$ loop of 2 bit multilevel STT MRAM corresponding to fabricated devices in Fig. 3(b). The MTJ size is set to be 40 nm in the simulation.

III. PROPOSED COMPOUND SPINTRONIC SYNAPSE AND NEURON

A. Compound Spintronic Synapse

Generally, each synapse in the ANNs is characterized by a weight, transmitting the weighted signal from its pre- to post-neuron. And an essential property of the synapse is its analog tunable synaptic weight. In the emerging field of the synaptic electronics, the synaptic weights can be characterized by the conductances of synaptic devices. Unfortunately, a MTJ device could only exhibit two stable conductance states. In order to exactly mimic the functionality of the synapse, the proposed compound spintronic device is employed to behave as a single synapse, termed as compound spintronic synapse (CSS). As a result, such CSS can achieve multiple discrete conductance states with well design and manipulation of materials/thickness of the capping layer and thickness of MgO tunneling barrier. With the number of MTJs in one CSS increasing, its conductance stats increase more rapidly, thus achieving an analog-like synaptic weight spectrum. It is worth noting that the generated current by the read voltage V_R of input neuron is required to be much smaller than the critical switching current of the MTJ nano-pillar to ensure that the synaptic weights cannot be changed during the transmission stage of the weighted signals.

In order to validate its feasibility, a CSS with three vertically stacked MTJs was simulated. The main parameters of these three MTJs in this simulation are shown in Table II. And the simulation results are shown in Fig. 5. As seen, such CSS can achieve 8 discrete resistance states. By generating different input current pulses, the proposed CSS can be set into a specific weight state as needed by the whole neuromorphic computation system. Additionally, the impact of device variations originated in the fabrication process is also taken into consideration. With

TABLE II
PARAMETERS AND VARIABLES PRESENT IN THE FITTING FUNCTIONS

Parameter	Description	Default value
Area	MTJ surface	40nm$*$40nm$*\pi/4$
TMR(0)	TMR ratio with zero V_{bias}	200%
t_f	Free layer height	1.3nm
V	Volume of free layer	Area*t_f
RA_1	Resistance*Area product of MTJ_1	$5\Omega \cdot \mu m^2$
RA_2	Resistance*Area product of MTJ_2	$10\Omega \cdot \mu m^2$
RA_3	Resistance*Area product of MTJ_3	$20\Omega \cdot \mu m^2$
I_{c1}	Critical switching current of MTJ_1	$50\mu A$
I_{c2}	Critical switching current of MTJ_2	$75\mu A$
I_{c3}	Critical switching current of MTJ_3	$100\mu A$

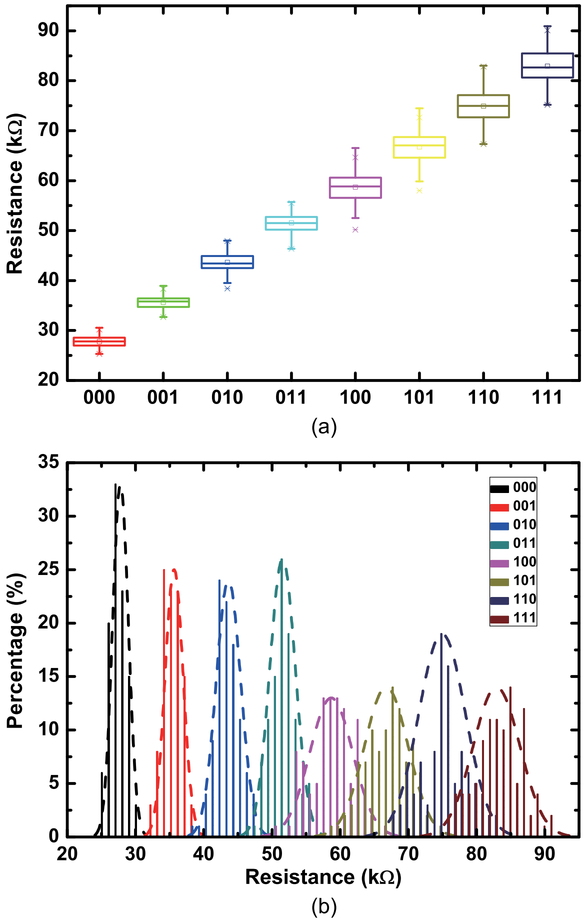


Fig. 5. Compound spintronic synapse (CSS) with 8 discrete synaptic weights. For the multilevel CSS, the impact of device variation on the resistance of separated synaptic states are also shown. The variation for temperature, MgO tunneling barrier thickness and TMR are set to be 3%. It is clear that even with such device variation, the CSS can achieve 8 distinct resistance levels.

5% variations for perpendicular magnetic anisotropy field H_k and resistance area product RA, well separated critical switching current and resistance states still can be achieved. It is worth noting that our proposed all spin artificial neural networks performs off-line learning paradigm (The training is performed by system-level simulation, then the simulated synaptic weights are mapped into CSSs discrete resistance states.). As a consequence, only variations in resistance area product RA which affects the separation of resistance states would have effect on the performance of neuromorphic computation system.

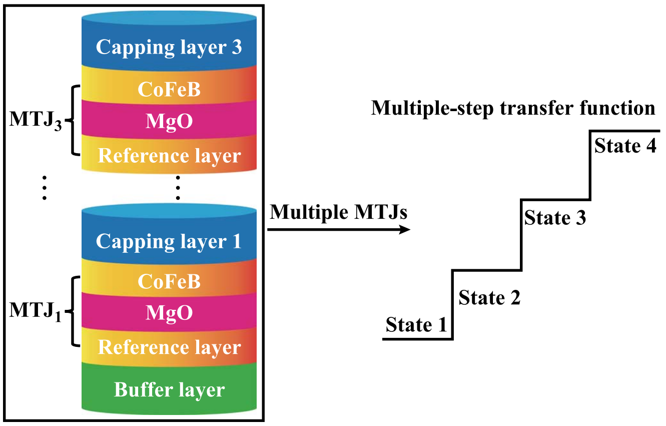


Fig. 6. Proposed compound spintronic neuron (CSN), which can implement a multiple-step transfer function.

B. Compound Spintronic Neuron

As the basic computational element in ANNs, each neuron is generally characterized by a transfer function (activation function). The neuron generates an output signal depending on the magnitude of the summation of its synaptic weighted input signals. And then the neuron's output signal is transmitted via the axon as the input of its fan-out neurons. In [28], a single MTJ device has been demonstrated to emulate the step transfer function (corresponding to the switching between its two stable states by a resultant synaptic current) in ANNs. Non-step (linear and sigmoid) transfer function could be more attractive for complex pattern recognition tasks since more information can be encoded in the neuron's output. For this, we proposed a compound spintronic neuron (CSN) that also employs multiple MTJs to function as a single neuron as shown in Fig. 6. Since vertically stacked MTJs can exhibit multiple discrete resistance states due to designed perpendicular magnetic anisotropy field H_k and resistance area product RA, analog-like information can be encoded in the CSN output to implement a multiple-step (linear-like) transfer function. It is worth noting that in case of CSN, $N+1$ steps for the transfer function can be implemented with N stacked MTJs, different from the 2^N discrete states for CSS.

To implement a multiple-step (linear-like) transfer function, a CSN circuit was proposed as shown in Fig. 7(a), which involves three operation phases, i.e., encode, read and reset phase. During the encode phase in Fig. 7(b), the NMOS transistor N1 turns on and the N2, N3 and the transmission gate (TG) are in off state. As a result, the resultant synaptic current, I_{synapse}, can be encoded into the CSN resistance state. Higher the magnitude of the resultant synaptic current I_{synapse}, higher resistance state the CSN can be switched into. Then, the CSN circuit enters the read phase as shown in Fig. 7(c). During it, the N2 and the TG turn on and the N1 and N3 are in off state. As a result, the CSN can generate a voltage signal V_{out} depending on its resistance state to the next layer neurons. Also, the output voltage signal V_{out} can be tuned by varying I_{read}. After the information is transferred to the next layer, the CSN circuit is reset for next operation as shown in Fig. 7(d). That is, all the MTJs are set to be in parallel configuration in reset stage. As a result, the

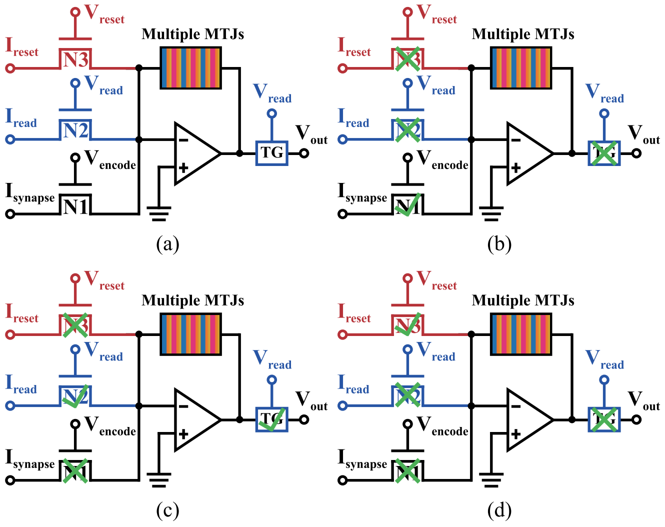


Fig. 7. Operation of the proposed compound spintronic neuron. (a) CSN circuit. (b) Encode phase. (c) Read phase. (d) Reset phase.

transfer function realized by the CSN can be characterized by the relationship of the I_{synapse} and the output voltage signal V_{out}.

To validate the functionality of the proposed CSN circuit, hybrid CMOS/MTJ circuit simulation was performed with the commercial CMOS 40 nm design kit. In the simulation, the CSN is composed of three vertically stacked MTJs as shown in Table II. Fig. 8(a) shows the relationship of the resultant synaptic current I_{synapse} of 10 ns and the resistance state of the CSN during the encode phase. As seen, the I_{synapse} can be encoded into four discrete resistance states of the CSN at 69/97/123 μA. For example, if the I_{synapse} is larger than 69 μA but smaller than 97 μA, the CSN is encoded in the "001" state. Fig. 8(b) shows the relationship of the output voltage signal V_{out} and the resistance state of the CSN, considering the variations for temperature, MgO tunneling barrier thickness and TMR of 3%. In the simulation, the I_{read} is set to be -1 μA to avoid the voltage bias effect on the resistance of the CSN.

IV. Proposed All Spin Artificial Neural Networks

A. *Structure of Proposed All Spin Artificial Neural Network*

Based on the proposed CSS and CSN, an all spin artificial neural network (ASANN) is proposed. It is designed as a fully connected feed-forward three-layer network. The network between the input and hidden layer as well as that between the hidden and output layer can be implemented by a crossbar architecture. Fig. 9 shows the network between the input and hidden layer, where each crosspoint consists of a CSS and its resistance state encodes the synaptic weight. Each input neuron generates a corresponding voltage depending on the training data. These input voltages are applied to the corresponding horizontal metal lines of the CSS crossbar. Then, these input voltages are modulated by the corresponding CSS in each vertical mental line, generating the weighted input signals (i.e., the synaptic currents). These weighted input signals are summed into the CSN circuit located at the end of each vertical mental

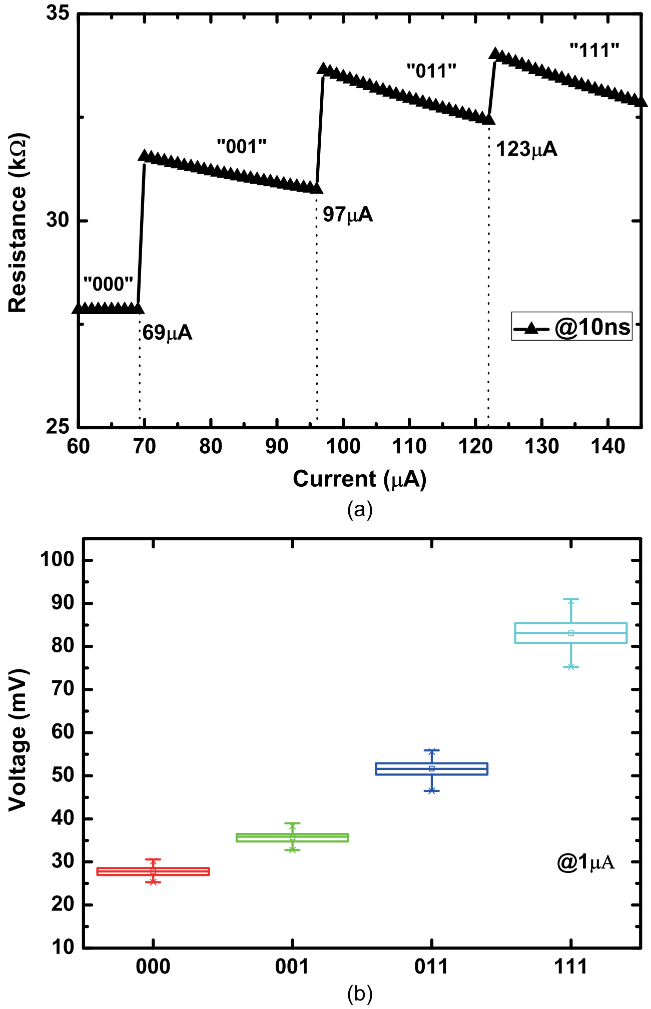


Fig. 8. (a) The simulated threshold switching current for different CSN resistance states and its resistance. 10 ns pulse is used for the simulation. (b) The output voltage of the CSN for different states. Device variations are considered in the simulation. Taken (a) and (b) together, the transfer function of the proposed CSN can be obtained.

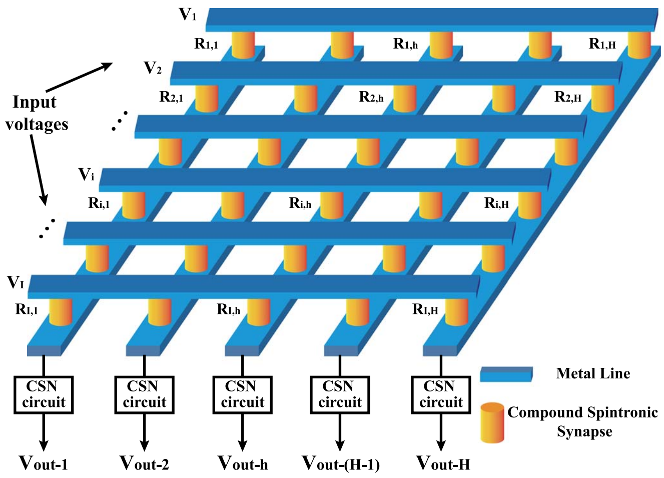
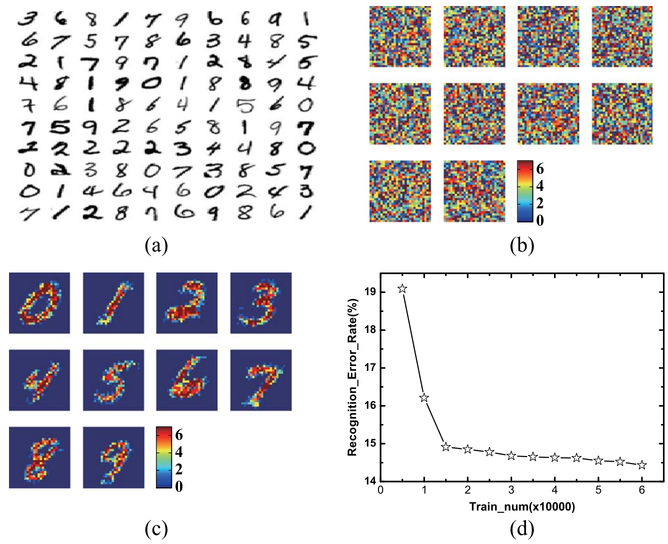


Fig. 9. The crossbar structure between the input and hidden layer with the proposed CSS and CSN circuit.



(a) (b) (c) (d)

Fig. 10. System-level simulation results. (a) Examples of digital patterns in the MNIST database. (b) Initialization of the synaptic weight matrix of the network between the input and hidden layer. (c) The learned handwritten digital patterns. (d) The recognition error rate during the training process.

line. In the encode phase of the CSN in hidden layer, the CSN is encoded into a specific resistance state according to the magnitude of the summed synaptic currents. Then, in the read phase of the CSN, the CSN outputs a voltage signal, whose magnitude depends on the resistance state of the corresponding CSN. And the output voltage signal is transferred to the network between hidden and output layer as a input signal. The network between hidden and output layer is the same as that in Fig. 9, and the output signals of the neurons in the output layer give the recognition result.

To investigate the performance of the proposed ASANN, a study case was made on the MNIST which is a widely used database for the handwritten digital recognition including 60 000 and 10 000 handwritten digital patterns for training and testing respectively [34]. Since there are 10 kinds of different handwritten digits in the database and each digit is composed of $28 * 28 = 784$ pixels with 256 level gray levels, the number of input neurons is set to be 784 and the number of output neurons is set to be 10. In order to more accurately learn all the handwritten digits, the number of the hidden neurons is set to 100. The network between the input and hidden layer was used to learn the handwritten digits and that between the hidden and output layer to classify the learned handwritten digits. The standard back-propagation algorithm was employed for the training process [34]. After the training process is completed, the trained weight of each synapse is mapped into our CSS crossbar network with discrete weight. Then recognition test will be performed on the proposed ASANN consisting of the CSS and CSN with real physical parameters listed in Table II. It is worth noting that the off-line learning is used since the back-propagation is easier for software implementation but more difficulty for hardware implementation.

Taking each CSS with 3 MTJs and each CSN with 1 MTJ for instance, Fig. 10 shows the simulation results. Fig. 10(a) shows the examples of the handwritten digits from the database. Initially, each CSS weight was set randomly as shown in Fig. 10(b). Fig. 10(c) shows the learned handwritten digital patterns. To quantitatively evaluate the learning accuracy of the proposed ASANN, Fig. 10(d) shows the recognition error rate during the training process. As can be seen, the recognition error rate could reach about 9.15%.

TABLE III
RECOGNITION ERROR RATE (RER) UNDER DIFFERENT RESOLUTION OF BOTH THE CSS WEIGHT AND CSN OUTPUT SIGNAL

RER CSS CSN	N=1	N=2	N=3
N=1	33.28%	20.51%	14.49%
N=2	32.19%	19.40%	13.26%
N=3	31.59%	18.62%	12.55%
Linear	30.01%	16.30%	9.73%

TABLE IV
THE INFLUENCE OF THE DEVICE VARIATION ON RECOGNITION ERROR RATE (RER) IN THE CASE OF THE CSN WITH 3 MTJs

RER CSS Var.	N=1	N=2	N=3
0	33.28%	20.51%	14.49%
10%	33.43%	20.71%	14.63%
20%	33.63%	21.77%	15.28%
30%	35.77%	24.02%	16.69%

B. Impact of the Resolution of Both the CSS Weight and CSN Output Signal on System Performance

It is worth noting that the number of the MTJs (N) in each compound spintronic device determines the resolution of both the CSS weight and CSN output signal. Apparently, the larger N, the higher is the learning accuracy of the proposed ASANN. Unfortunately, higher N would increase the difficulty of device fabrication and energy dissipation. To investigate the impact of the low resolution of the CSS weight and CSN output signal on the learning accuracy of the proposed ASANN, we repeated the simulation in the above subsection. The simulation results for varying the number of the MTJs in both the CSS and CSN are shown in Table III. As we can see, obviously higher resolution of the CSS weight and CSN output signal resolution leads to lower recognition error rate. Detailed analysis shows that the weight resolution of the CSS has a more significant influence on the learning accuracy of the proposed ASANN than that of the CSN output signal. This implies different roles of the CSS weight and CSN output signal resolution in the proposed ASANN.

C. Impact of the Device Variation on System Performance

For large scale implementation of the proposed compound spintronic device, there exist massive device variation on its resistance in different states, which will directly influence the CSS weight. In the following, the impact of device variation on the recognition error rate was investigated. By performing the circuit-level Monte Carlo simulation, the distributions of the resistance of the CSS in different states were obtained. Then, the simulation in the above subsection was repeated with different CSS weight resolutions, where the CSN was with 3 MTJs. Simulation results are shown in Table IV. We can observe that the larger device variation results in the larger recognition error rate. That is, it can degrade the accuracy of neuromorphic computation. Fortunately, the higher the weight resolution, the greater tolerance the neural network system has.

V. Conclusion

In this paper, an all spin artificial neural network (ASANN) is constructed with the proposed compound spintronic synapse (CSS) and neuron (CSN). Both the CSS and CSN are based on a compound spintronic device, which consists of multiple vertically stacked MTJs. From the views of the device physics, fabrication and circuit-level simulation, we have demonstrated that the proposed CSS and CSN can achieve multiple discrete weight levels and implement a multi-step transfer function, respectively. Additionally, the performance of the built ASANN has been investigated by performing system-level simulations with off-line training on the MNIST database for handwritten digital recognition. Moreover, the impact of both the resolution of the proposed CSS and CSN and device variation on system performance has also been evaluated. It has been proved that the proposed CSS and CSN can be employed to build the next generation neural computation platform. However, more physical evaluation and fabrication work will be taken in the future research work.

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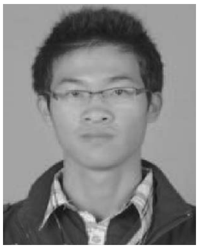

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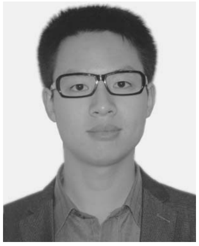

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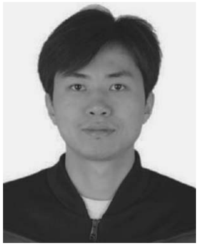

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