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Memristor-Based Efficient In-Memory Logic for Cryptologic and Arithmetic Applications

Liying Xu, Rui Yuan, Zhenhua Zhu, Keqin Liu, Zhaokun Jing, Yimao Cai, Yu Wang, Yuchao Yang, and Ru Huang**

As the era of big data dawns, conventional digital computers face increasing difficulties in performance and power efficiency due to their von Neumann architecture, leading to an urgent requirement for computing paradigms that can merge logic and memory. An efficient in-memory logic approach based on unipolar memristors that is capable of implementing all 16 Boolean logic functions in the same cell in less than 3 logic steps using a thermochemical metallization cell, where the confinement of filament diameter and thus switching location have reduced the threshold voltages and improved the switching uniformity, is experimentally demonstrated. The high efficiency of the logic units allows for the construction of novel encryption hardware in which both the encryption and decryption processes are achieved by memristor logic while the encryption key is also generated from the intrinsic stochasticity of resistive switching. The memristive array is also used to implement the calculation of Hamming distance and 1-bit binary full adder with high efficiency, thus paving a way for future non-von Neumann computing architectures.

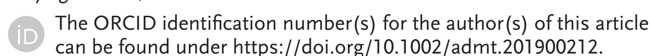
1. Introduction

Having dominated the computing market for over half a century, conventional digital computers are up to a radical shift from the traditional von Neumann architecture. On the one hand, the feature size of traditional CMOS component is approaching its physical limitation, implying that continued enhancement of computing performance is unlikely to further benefit from scaling. On the other hand, the ceaseless data transfer between the logic and memory units is becoming even more of a severe issue nowadays in terms of performance and energy efficiency, due to the rapid explosion of data volume recently. For example, over 30 ZB of new data were produced in 2018 around the world, and the data centers and consumer electronics have cost >10% of global electric supply.[1] As a result, it is an imperative task to develop a new generation of data-centric computing architecture, in order to meet the constantly increasing requirements on energy efficiency. In-memory logic, also named nonvolatile logic or processing in memory (PIM), is one of the most promising candidates for future non-von Neumann architectures, where the logic operation can be executed in memory device itself, thereby eliminating the von Neumann bottleneck from the device level and potentially leading to improved energy efficiency.[2,3]

Recently, dramatic efforts have been dedicated to the investigation of in-memory logic based on memristors, due to their high speed, high scalability, nonvolatile nature, and low energy consumption,[4–8] and have demonstrated rich logic functionalities.[9–23] Most of the existing studies on memristor-based logics are based on devices with bipolar resistive switching (BRS),[11–18] although some attention was paid to logic implementations using devices with complementary resistive switching (CRS)[18,20–22] or unipolar resistive switching (URS)[24–26] as well. In light of the physical quantities that are used to represent the logic inputs and outputs in the logic cells, memristor logics can be roughly categorized into two classes—stateful and nonstateful logic. In the former case, the resistance (conductance) states of the memristive devices involved are used as both the input and output variables, e.g., in IMPLY[11] and MAGIC.[12] Instead, the stimulation signals applied on the devices are adopted as the input variables in nonstateful logic, while the device resistance still serves as the output.[18] Generally, stateful logics require a larger number of devices in a dedicated logic gate, and the Boolean logic functions that can be realized using the same circuit configuration are usually limited, hence leading to low reconfigurability. The advantage of stateful logic lies in the fact that the logic cascading is straightforward, given the identical nature of input and output variables. On the contrary, nonstateful logics usually require a smaller number of devices for a logic gate, and the reconfigurability of the logic circuits can be defined by the

L. Xu, R. Yuan, K. Liu, Z. Jing, Prof. Y. Cai, Prof. Y. Yang, Prof. R. Huang
National Key Laboratory of Science and Technology
on Micro/Nano Fabrication
Institute of Microelectronics
Peking University
Beijing 100871, China
E-mail: yuchaoyang@pku.edu.cn; ruhuang@pku.edu.cn

Z. Zhu, Prof. Y. Wang
Department of Electronic Engineering
Beijing National Research Center for Information Science
and Technology (BNRist)
Tsinghua University
Beijing 100084, China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input signals and is thus much higher. However, additional processing is generally needed before logic cascading can be done, due to the different nature of the input and output variables, e.g., voltage versus resistance. Obviously, there is a tradeoff between device number, reconfigurability, and ease of logic cascading, and the overall efficiency of stateful and nonstateful logics remains a controversy. The research community is still pursuing an in-memory logic approach with high efficiency and high logic completeness. Besides, continued advancement of in-memory logic technology requires scaling up of the logic cells and demonstration of more practical applications at the array level.

In this study, we present an in-memory logic approach based on unipolar memristors, which can realize all 16 Boolean logic functions in less than 3 steps, using an optimized Ta_2O_5 memristor cell, where the confinement of filament diameter and thus switching location have reduced the threshold voltages and improved the uniformity of the devices. The high efficiency of the memristor logic herein has allowed us to construct a novel encryption system, in which both the encryption and decryption are performed by the XOR logic in memristors and the encryption key is generated from the intrinsic stochasticity of resistive switching. The calculation of Hamming distance and 1-bit binary full adder are also experimentally demonstrated with high efficiency. This in-memory logic approach therefore offers a promising candidate for future cryptologic and arithmetic applications.

2. Optimization of Ta_2O_5-Based Memristors via Filament Confinement

Figure 1a schematically illustrates the structure of a $Pd/Ta_2O_5/Pd$ unipolar device fabricated on SiO_2/Si substrates (see the Experimental Section for fabrication details), and the inset shows a top-view optical microscopy image for the crossbar array, where the size of the crosspoint is 2 × 2 µm^2. The stacking structure of the device can be clearly observed from a cross-sectional transmission electron microscopy (TEM) image shown in Figure 1b, and the compositions of each layer were verified by detailed energy dispersive X-ray spectroscopy (EDS) line scan and mapping characterization, as shown in Figure 1c,d. Figure 1e shows typical resistive switching characteristics of the $Pd/Ta_2O_5/Pd$ devices. A forming process with a voltage of ≈6.5 V was needed to initialize pristine devices, where a current compliance (CC) of 10 µA was used to prevent

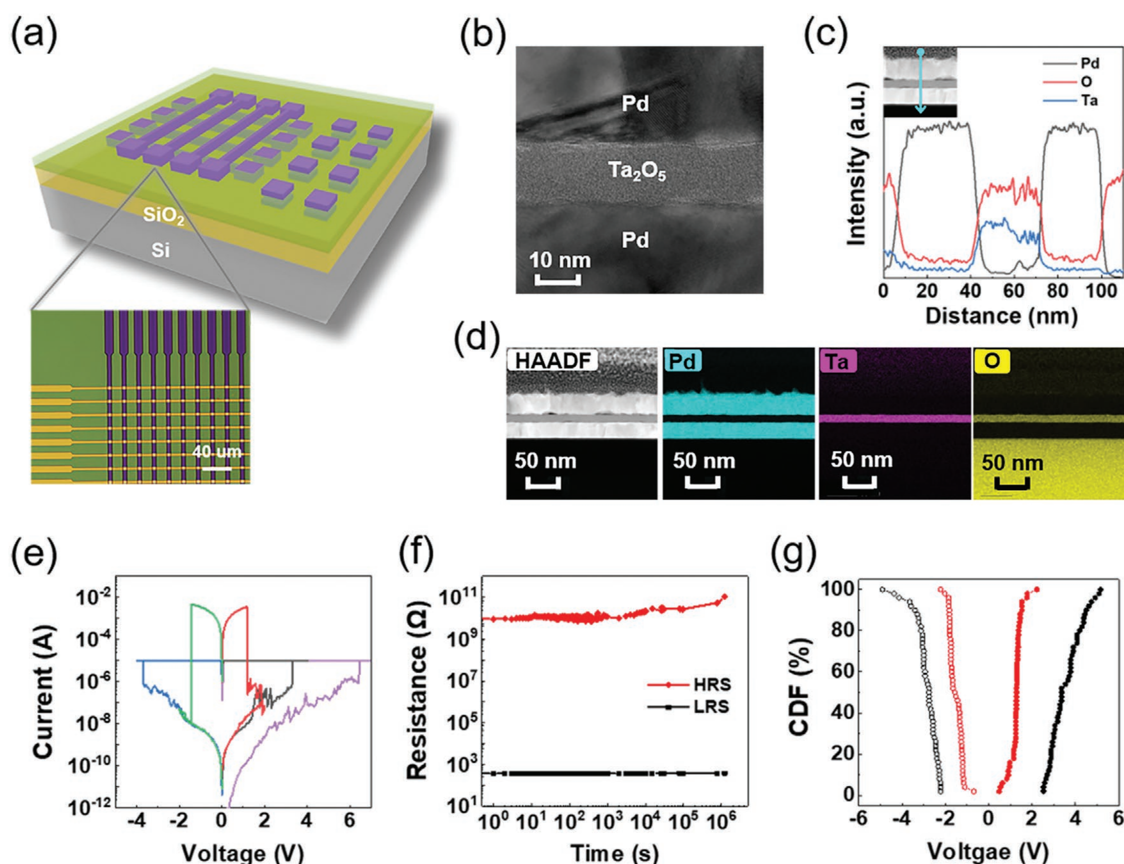

Figure 1. Characterization of Ta_2O_5-based unipolar memristors. a) Schematic illustration of the device structure. The image (lower position) shows the particle top views of devices by optical microscope. Scale bar: 40 µm. b) Cross-section TEM image of the $Pd/Ta_2O_5/Pd$ structure. Scale bar: 10 nm. c) EDS line scan (the inset shows the scan direction), and d) EDS mapping on cross-section of $Pd/Ta_2O_5/Pd$ device for compositional analysis. Scale bar: 50 nm. e) Typical resistive switching characteristics of the $Pd/Ta_2O_5/Pd$ devices. f) The retention characteristic of HRS and LRS. g) Cumulative distributions of threshold voltages for $Pd/Ta_2O_5/Pd$ device. The hollow circles represent the negative threshold voltages, and the solid circles indicate the positive threshold voltages. The set threshold voltages are marked with black color, and the reset threshold voltages are marked with red color.

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hard breakdown (Figure 1e). Subsequently, reproducible resistive switching can be achieved by applying a set voltage of 3.3–3.7 V and a reset voltage of 1.2–1.5 V regardless of the voltage polarity, showing typical unipolar resistive switching behavior with a high on–off ratio of $>10^6$ (Figure 1e). The large difference existing in the amplitudes of $|V_{set}|$ and $|V_{reset}|$ as well as in the resistance values of high resistance state (HRS) and low resistance state (LRS) in unipolar devices are beneficial for the reliability of logic operations. Figure 1f further shows that the HRS and LRS of the $Pd/Ta_2O_5/Pd$ memristors remain stable for $>10^6$ s without noticeable degradation, indicating a nonvolatile nature that is needed for in-memory logic. The cumulative probability distribution of device resistance in both on and off states can be found in Figure S1a in the Supporting Information. However, the $Pd/Ta_2O_5/Pd$ devices can only be switched using DC sweeps owing to low operation speed (typically seconds), which practically prevents realization of logic functions using electric pulses. This is expected to originate from the formation of a robust conducting filament in the $Pd/Ta_2O_5/Pd$ structure. Indeed, a strong cone-shaped filament has been reported in Pt/CuO/Pt[27] and $Pt/TiO_2/Pt$[28] devices with a similar stacking structure consisting of symmetric, inert electrodes, and a single switching oxide in between. Such strong cone-shaped filaments without apparent weak points determine that both the growth and dissolution processes are retarded, and the adoption of inert Pt or Pd as both electrodes is also unfavorable for efficient oxygen exchange between the electrodes and the switching medium.

In order to address the above issue, we have introduced a SiO_2 layer (3 nm) into the switching medium by inserting it between two Ta_2O_5 layers (10 nm), thus forming a $Ta_2O_5/SiO_2/Ta_2O_5$ trilayer. It has been reported that SiO_2 is characteristic of lower oxygen diffusion rate compared with Ta_2O_5, which may retard the oxygen migration and overall filament growth therein.[29,30] As a result, the diameter of the filament is expected to be smaller in the SiO_2 layer compared with that in the upper and lower Ta_2O_5 layers, thus implying an hourglass-shaped filament (**Figure 2**a). Since the filament growth and dissolution are mainly driven by Joule heating in unipolar memristors, the small filament diameter in SiO_2 decides that the current density and thus the thermal effects therein are most significant, which in turn lead to the confinement of filament growth/dissolution in the SiO_2 layer.[31,32] The previous Pd electrodes were also replaced by TiN, a material normally utilized as an oxygen vacancy reservoir. Therefore, the efficiency of oxygen exchange between the electrodes and the switching medium will also be enhanced. Such confined filament size and enhanced oxygen exchange are expected to facilitate resistive switching in the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices. Figure 2b,c shows cross-sectional TEM image and EDS line scan analysis of the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices, which clearly shows the device structure with an oxide trilayer. Notably, the EDS line profiles suggest possible existence of a very thin TiO_xN_y layer at each TiN/Ta_2O_5 interface (Figure 2c). This will oxidize the original Ti^{3+} ions in TiN to higher valence state[33] and at the same time increase the oxygen vacancy concentrations in Ta_2O_5, which is expected to facilitate the forming and switching processes. The EDS mapping analysis on the cross-section can be found in Figure S1b in the Supporting

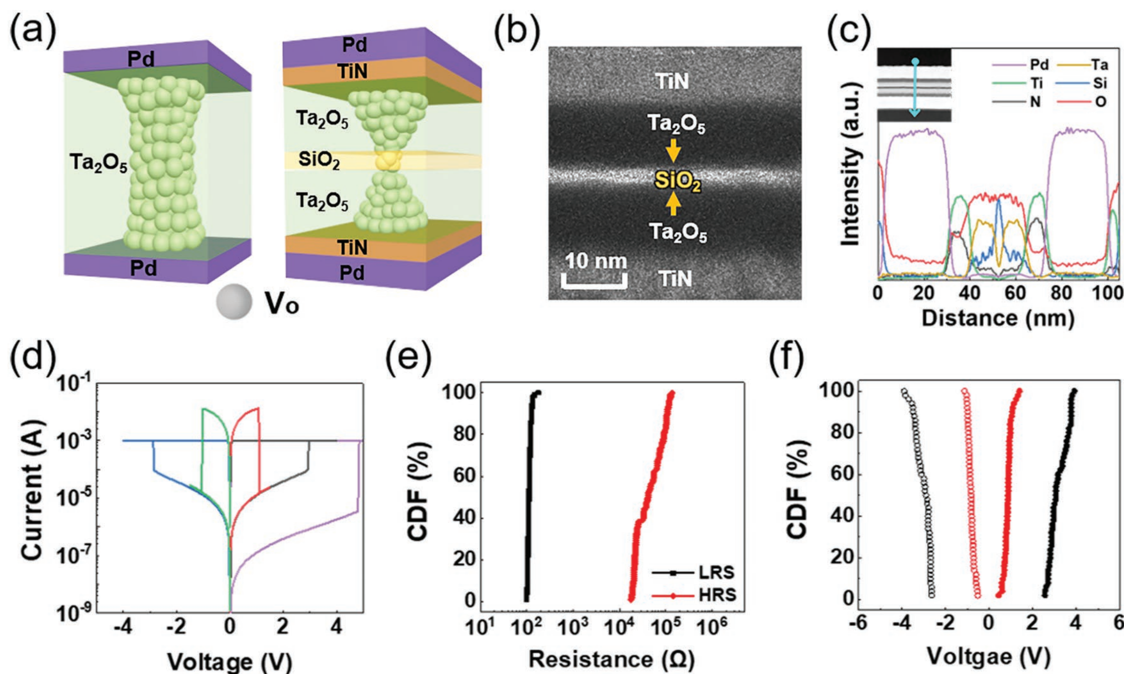

Figure 2. a) Schematic illustration of conducting filaments formed in the $Pd/Ta_2O_5/Pd$ structure and the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ structure. b) Cross-sectional TEM image of the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ structure. Scale bar: 10 nm. c) EDS line scan on the cross-section of $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ device for compositional analysis. Scale bar: 50 nm. d) Typical resistive switching characteristics of the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices. e) Cycle-to-cycle cumulative distributions of HRS and LRS in the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices. f) Cumulative distributions of threshold voltages for $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ device. The hollow circles represent the negative threshold voltages, and the solid circles indicate the positive threshold voltages. The set threshold voltages are marked with black color, and the reset threshold voltages are marked with red color.

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Information. Figure 2d further shows the resistive switching characteristics of the trilayer devices, where unipolar switching is once again obtained. One can see that the forming, set, and reset voltages in the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices are reduced to ≈5, 2.9–3, and ≈1.1 V, respectively, and the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices can be reliably switched in pulse mode, in agreement with the easier filament growth and dissolution due to the confined filament size. Further characterization on the operation speed of $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices showed that the widths of set and reset pulses can be reduced to 100 ns and 1 ms, respectively (Figure S2, Supporting Information), while continued optimization on the operation speed (and device currents) could be achieved by adjusting the thickness of the SiO_2 layer and scaling the cell size to nanometer dimensions. Control experiments revealed an independence of the on-state resistance on electrode area (Figure S3, Supporting Information), therefore consistent with the filamentary picture. It is expected that the existence of moisture in ambient conditions also plays a role in the forming process of both types of devices, by providing a reduction reaction at the cathodic interface to compensate the charge of oxygen vacancies generated during forming.[34,35] Figure 2e further shows the cumulative probability distribution of device resistance in the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ memristors, where good uniformity can be observed in the resistance of both on and off states (see cumulative probability distribution of the $Pd/Ta_2O_5/Pd$ devices in Figure S1a in the Supporting Information). This can once again be ascribed to largely fixed location of filament growth/dissolution, due to the hourglass geometry of the filament in the $Ta_2O_5/SiO_2/Ta_2O_5$ trilayer. The uniformity of set/reset voltages is another crucial parameter for logic applications. Figures 1g and 2f show the cumulative distributions of the threshold voltages in $Pd/Ta_2O_5/Pd$ and $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ unipolar devices, respectively. It is obvious that the uniformity of set/reset threshold voltages is improved in $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices, which can be attributed to the filament confinement in the SiO_2 layer, making them better candidates for robust logic operations. While the inclusion of SiO_2 in the switching medium plays a key role in improving the uniformity of resistive switching in terms of both resistance distribution and threshold voltages, the TiN electrode also contributes to the reduced threshold voltages and improved stability in $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices. It is worthwhile pointing out that herein SiO_2 is adopted only as an intermediate layer confining the size of the filament, but Ta_2O_5 still serves as the major switching medium and is mainly responsible for the resistive switching phenomenon observed.

3. Experimental Realization of All 16 Boolean Logic Functions

We now turn to the implementation of in-memory logic based on unipolar devices. **Figure 3**a shows the definition of logic inputs and output in the devices, where the voltage signals applied on the two terminals (T_1, T_2) represent the inputs and the final resistance state Z of the memristor represents the output, thus falling into nonstateful logic category.

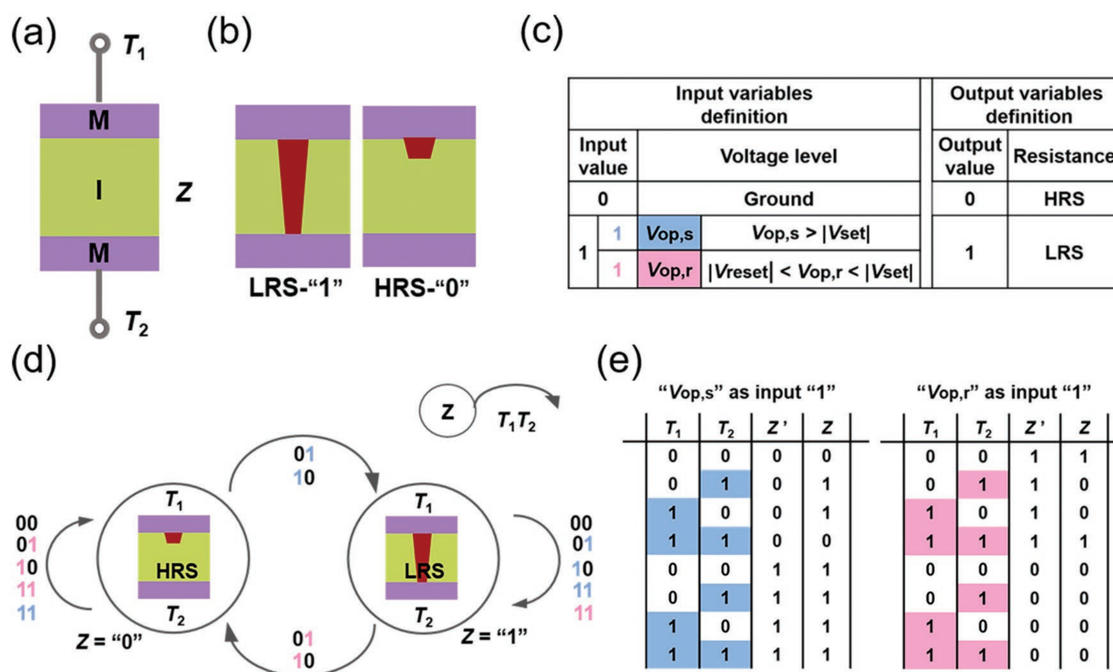

Figure 3. Logic definition based on the unipolar memristors. a) Typical sketch of two terminal memristor. T_1, T_2 represent the logic inputs applied to the two terminals and Z represents the device state. b) Definition of logic output, i.e., HRS as logic "0" and LRS as logic "1". c) Logic definitions of input and output variables. For input variable "1", two definition modes are marked in blue and pink and can be flexibly selected, leading to different logic functions. d) The finite state machine of unipolar memristors for logic definition. e) Truth tables for logic operation in unipolar memristors based on the two definitions for logic input "1". The logic input "1" marked with blue color indicates "$V_{op,s}$", and the logic input "1" marked with pink color indicates "$V_{op,r}$".

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Furthermore, HRS is defined as logic "0" and LRS is defined as logic "1", as shown in Figure 3b. Obviously, the final resistance state (Z) is a function of the initial device state (Z') and the applied signals (T_1, T_2). In-memory logic is naturally realized because the device resistance is directly stored in the device itself after logic operations. Since set and reset voltages are distinguished by their amplitudes, the logic input can be further divided into $V_{op,s}$ ($V_{op,s} \geq |V_{set}|$) that can switch the device to LRS and $V_{op,r}$ ($|V_{reset}| \leq V_{op,r} < |V_{set}|$) that can switch the device to HRS. Figure 3c summarizes the definition of the logic variables in detail, and the corresponding finite state machine can be illustrated in Figure 3d. When the initial state of the device is HRS (Z' = "0"), combined inputs T_1T_2 of "10" or "01" (where $V_{op,s}$ is used as "1") will be able to switch the device to LRS (Z = "1"), which naturally realizes the XOR function, i.e., $Z = T_1$ XOR T_2. This is however very difficult for existing memristor logic approaches. While the implementation of XOR function based on a stateful approach requires more memristive cells,[36] the XOR logic in a single bipolar memristor includes the initialization step or control signal as additional input variable,[37] and conditional reading operations are needed to implement XOR in switchable diodes[19] and complementary resistive switches.[21,22] When the initial state of the device is HRS (Z' = "1"), combined inputs T_1T_2 of "10" or "01" (where $V_{op,r}$ is used as "1") can switch the device to HRS (Z = "0"), thus implementing the XNOR function, i.e., $Z = T_1$ XNOR T_2. This function is once again challenging for existing memristor logics,[18,19,21,22] showing the advantage of the present approach. Figure 3e shows the truth tables for the two cases, which can be described by Equation (1) where $V_{op,s}$ is adopted as input "1" and Equation (2) where $V_{op,r}$ is adopted as input "1"

$$Z = \text{TRUE} \cdot Z' + (T_1 \text{ XOR } T_2) \cdot \text{NOT } Z' \tag{1}$$

$$Z = (T_1 \text{ XNOR } T_2) \cdot Z' + \text{FALSE} \cdot \text{NOT } Z' \tag{2}$$

The electric signals applied on the two terminals T_1 and T_2 can be directly mapped as input variables p and q. For example, if "$T_1 = p$, $T_2 = q$, and $Z' = 0$", the logic expression (1) will be changed to Equation (3), provided that $V_{op,s}$ is adopted as input "1". Similarly, if "$T_1 = p$, $T_2 = q$, and $Z' = 1$", Equation (2) will be changed to Equation (4), if $V_{op,r}$ is adopted as input "1"

$$Z = \text{TRUE} \cdot 0 + (p \text{ XOR } q) \cdot 1 = p \text{ XOR } q \tag{3}$$

$$Z = (p \text{ XNOR } q) \cdot 1 + \text{FALSE} \cdot 0 = p \text{ XNOR } q \tag{4}$$

One can see that the above equations are exactly the XOR and XNOR functions. Furthermore, all the 16 Boolean logic functions can be realized by sequentially conducting the above logic operations in no more than 3 cycles. As an example, Equations (5)–(7) show the implementation of the NAND function. The unipolar memristor is first initialized to the HRS (Z' = "0") with "$T_1 = V_{op,r}$, $T_2 = 0$ (Ground)", and then "$T_1 = p$, $T_2 = 1$" are applied on the electrode pair to realize NOT p. Finally, "$T_1 = q$, $T_2 = 1$" are applied and p NAND q can be realized

$$Z_{\text{cycle1}} = 0 \tag{5}$$

$$\begin{aligned} Z_{\text{cycle2}} &= \text{TRUE} \cdot Z_{\text{cycle1}} + (T_1 \text{ XOR } T_2) \cdot \text{NOT } Z_{\text{cycle1}} \\ &= \text{TRUE} \cdot 0 + (p \text{ XOR } 1) \cdot 1 = \text{NOT } p \end{aligned} \tag{6}$$

$$\begin{aligned} Z_{\text{cycle3}} &= \text{TRUE} \cdot Z_{\text{cycle2}} + (T_1 \text{ XOR } T_2) \cdot \text{NOT } Z_{\text{cycle2}} \\ &= \text{TRUE} \cdot \text{NOT } p + (q \text{ XOR } 1) \cdot p = p \text{ NAND } q \end{aligned} \tag{7}$$

Table 1a further lists Boolean logic functions and corresponding logic sequences that can be derived from Equation (1), where the device should be initialized to HRS (Z' = "0") except for the TRUE function and $V_{op,s}$ acts as input value "1" for p and q. Table 1b lists the Boolean logic functions and corresponding logic sequences that can be derived from Equation (2), where the device should be initialized to LRS (Z' = 1) except for the FALSE function and $V_{op,r}$ acts as input value "1" for p and q. As a result, by simply configuring the definition of logic input "1" between two voltage amplitudes, all the 16 fundamental Boolean logic functions can be implemented in a single unipolar memristor in no more than 3 cycles, hence exhibiting superior performance in terms of efficiency, area, and logic completeness. We have experimentally implemented all the above 16 Boolean logic functions, as can be found in **Figure 4** and Figure S4 in the Supporting Information. Figure 4 shows experimental results from both DC and pulse operations, taking XOR and NAND functions as examples, while measurements on the other Boolean functions can be found in Figure S4 in the Supporting Information. It should be pointed out that herein the realization of all 16 Boolean logic functions in a single unipolar device without inclusion of selectors or diodes has advantages in logic completeness and structural as well as operational simplicity. However, in large-scale arrays where the crosstalk problem influences functional correctness or state read-out, the inclusion of selectors might be necessary. Based on the 16 basic Boolean logic functions, more practical and complex logic functions can be efficiently implemented in the array based on such unipolar memristors, as will be shown afterward.

4. Efficient Calculation of Hamming Distance Based on Memristor Logic

The implementation of XOR logic is cumbersome in conventional CMOS circuits as well as existing memristive logic. Since the XOR function plays an important role in a large number of arithmetic calculations, the present memristor logic approach can be utilized to realize efficient logic functions in practical applications, for example, the calculation of Hamming distance, as schematically shown in **Figure 5**a. Hamming distance is an effective method to calculate the feature distance and has been applied in extensive occasions such as communication coding and machine learning, which can be expressed as the number of different bits at corresponding positions for two bitstreams with equal length.[38] Namely, for two N-bit binary strings "$A_nA_{n-1}...A_i...A_2A_1$" and "$B_nB_{n-1}...B_i...B_2B_1$", the Hamming distance is equal to the number of "1" in the result of "A XOR B". Figure 5b shows a 16 × 16 unipolar memristor array that was used to experimentally calculate the Hamming distance of two 16-bit bitstreams "1111001100101100" and "0010100110101001". Voltage pulses representing the two bitstreams "1111001100101100" ("0010100110101001") were

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Table 1. Logic sequence for basic Boolean logic functions with a) the voltage signal "$V_{op,s}$" as input value "1", and b) the voltage signal "$V_{op,r}$" as input value "1".

(a)

Logic	Input		Terminal	Cycle			Read current			Output
	p	q		1	2	3	1	2	3	Z
TRUE	0	1	T_1	1			H			1
	0	1					H			1
	1	0	T_2	0			H			1
	1	1					H			1
p	0	0	T_1	Vop,r	p		L	L		0
	0	1					L	L		0
	1	0	T_2	0	0		L	H		1
	1	1					L	H		1
q	0	0	T_1	Vop,r	q		L	L		0
	0	1					L	H		1
	1	0	T_2	0	0		L	L		0
	1	1					L	H		1
NOT p	0	0	T_1	Vop,r	p		L	H		1
	0	1					L	H		1
	1	0	T_2	0	1		L	L		0
	1	1					L	L		0
NOT q	0	0	T_1	Vop,r	q		L	H		1
	0	1					L	L		0
	1	0	T_2	0	1		L	H		1
	1	1					L	L		0
XOR	0	0	T_1	Vop,r	p		L	L		0
	0	1					L	H		1
	1	0	T_2	0	q		L	H		1
	1	1					L	L		0
OR	0	0	T_1	Vop,r	p	q	L	L	L	0
	0	1					L	L	H	1
	1	0	T_2	0	0	0	L	H	H	1
	1	1					L	H	H	1
NAND	0	0	T_1	Vop,r	p	q	L	H	H	1
	0	1					L	H	H	1
	1	0	T_2	0	1	1	L	L	H	1
	1	1					L	L	L	0
IMP	0	0	T_1	Vop,r	p	q	L	H	H	1
	0	1					L	H	H	1
	1	0	T_2	0	1	0	L	L	L	0
	1	1					L	L	H	1
RIMP	0	0	T_1	Vop,r	p	q	L	L	H	1
	0	1					L	L	L	0
	1	0	T_2	0	0	1	L	H	H	1
	1	1					L	H	H	1

(b)

Logic	Input		Terminal	Cycle			Read current			Output
	p	q		1	2	3	1	2	3	Z
FALSE	0	1	T_1	1			L			0
	0	1					L			0
	1	0	T_2	0			L			0
	1	1					L			0
p	0	0	T_1	Vop,s	p		H	L		0
	0	1					H	L		0
	1	0	T_2	0	1		H	H		1
	1	1					H	H		1
q	0	0	T_1	Vop,s	q		H	L		0
	0	1					H	H		1
	1	0	T_2	0	1		H	L		0
	1	1					H	H		1
NOT p	0	0	T_1	Vop,s	p		H	H		1
	0	1					H	H		1
	1	0	T_2	0	0		H	L		0
	1	1					H	L		0
NOT q	0	0	T_1	Vop,s	q		H	H		1
	0	1					H	L		0
	1	0	T_2	0	0		H	H		1
	1	1					H	L		0
XNOR	0	0	T_1	Vop,s	p		H	H		1
	0	1					H	L		0
	1	0	T_2	0	q		H	L		0
	1	1					H	H		1
NOR	0	0	T_1	Vop,s	p	q	H	H	H	1
	0	1					H	H	L	0
	1	0	T_2	0	0	0	H	L	L	0
	1	1					H	L	L	0
AND	0	0	T_1	Vop,s	p	q	H	L	L	0
	0	1					H	L	L	0
	1	0	T_2	0	1	1	H	H	L	0
	1	1					H	H	H	1
NIMP	0	0	T_1	Vop,s	p	q	H	L	L	0
	0	1					H	L	L	0
	1	0	T_2	0	1	0	H	H	H	1
	1	1					H	H	L	0
RNIMP	0	0	T_1	Vop,s	p	q	H	H	L	0
	0	1					H	H	H	1
	1	0	T_2	0	0	1	H	L	L	0
	1	1					H	L	L	0

thus fed into the rows (columns) of the crossbar array, where $V_{op,s}$ acts as input value "1", and the devices located at the diagonal of the array are actively involved in the calculation. No forming process was performed to the rest of the devices in the array, so the applied voltage amplitude is insufficient to result in any switching events and prevent them from any disturbance during the calculation. Figure 5c shows the distribution of device states after initialization, where all the diagonal

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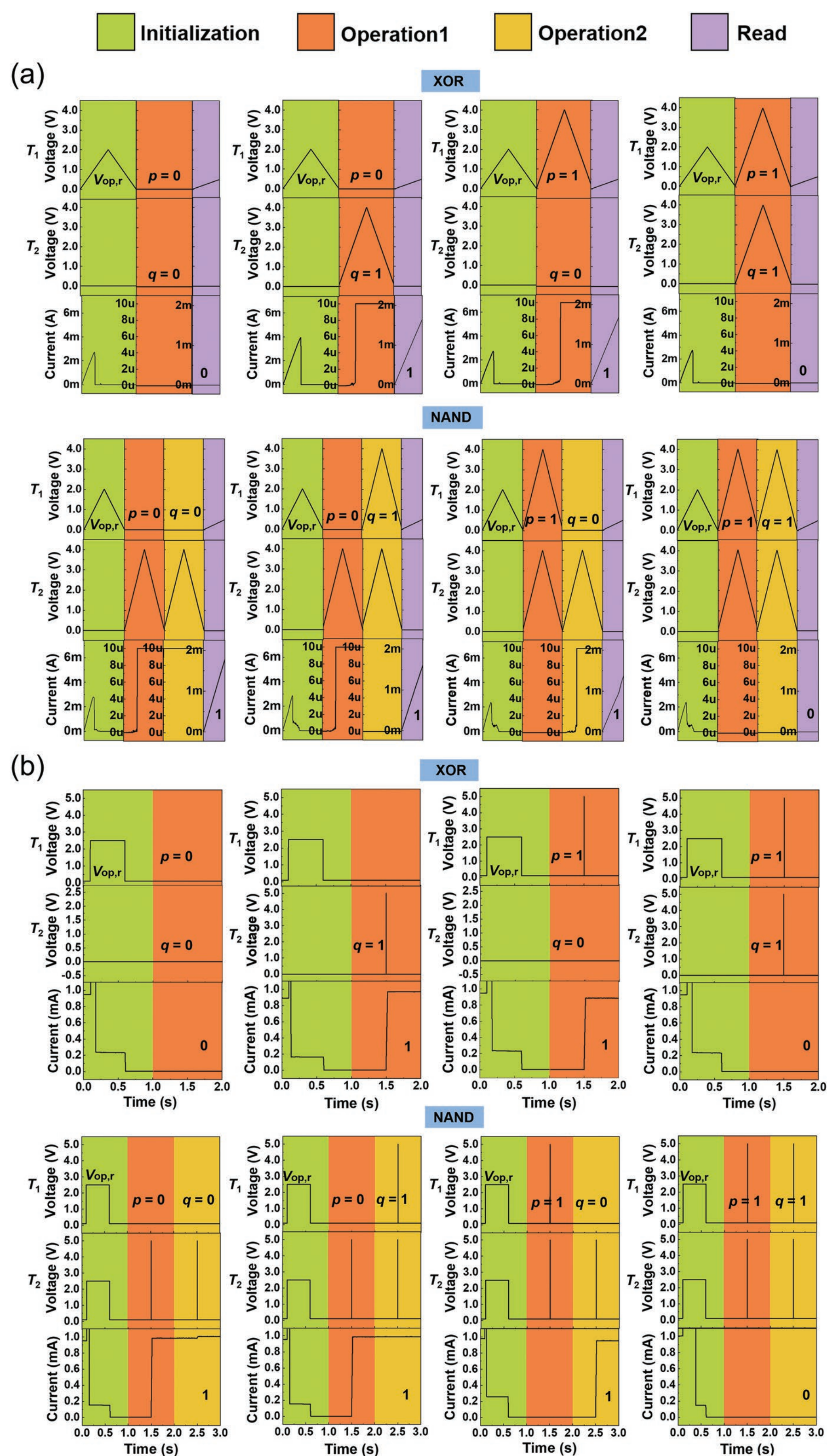

Figure 4. Experimental demonstration of XOR and NAND functions in DC and pulse measurements. a) DC measurements showing the implementation of the XOR and NAND functions. The initialization step (green background) was first performed. Then, one logic operating step (orange background) for XOR logic and two logic operating steps (orange and yellow background) for NAND logic were executed. The current is taken as its absolute value using voltage sweep up to 0.5 V (purple background). b) Pulse measurements showing the implementation of the XOR and NAND functions. Constant read voltage of 0.1 V was applied on the terminal T_1 during the entire logic operations.

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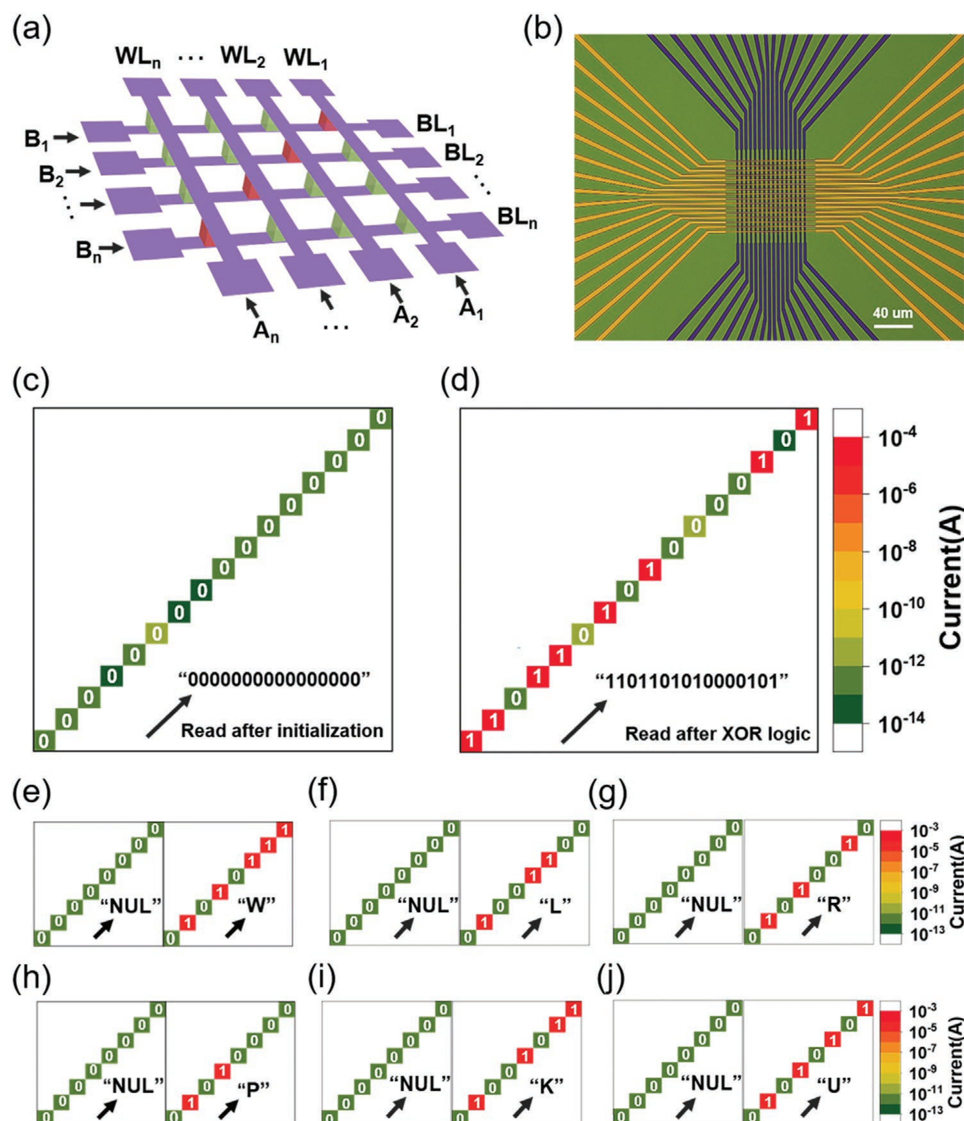

Figure 5. Unipolar memristive array for calculation of Hamming distance and hardware encryption. a) Schematic of $N \times N$ unipolar crossbar array for calculation of Hamming distance. The devices located at selected diagonal marked with red color can be used for XOR logic in parallel. b) Optical micrograph of 16×16 unipolar memristive array. Scale bar: 40 µm. c) The read current of diagonal devices after the initialization step. All devices located at the selected diagonal were initialized to HRS. d) The read current of diagonal devices after calculation of Hamming distance. Correct output "1101101010000101" was obtained, suggesting a Hamming distance of 8. e–j) The read current of diagonal devices after the initialization step (left part) and logic operation (right part) for e) encryption of "P", f) encryption of "K", and g) encryption of "U", and for h) decryption of "P", i) decryption of "K", and j) decryption of "U". The read voltage was 0.05 V. The arrows in (c)–(j) indicate that the direction from lower left to upper right corresponds to decrease of the bit significance.

devices showed HRS, and Figure 5d further presents the states of the diagonal devices after operation. One can see resistance distribution of "1101101010000101" was successfully obtained in the array, suggesting a Hamming distance of 8, which is the correct output.

5. Hardware Encryption Based on Memristor Arrays

Aside from the calculation of Hamming distance, the XOR operation has a unique feature: the output will return to its original value, if we execute the XOR operation twice. That is, if "A XOR $B = C$", then we can get "C XOR $B = A$". This feature forms the basis of symmetric encryption and decryption based upon the XOR logic, which is a simple and effective method to ensure information security. In this case, the plaintext represents the message before encryption, and the ciphertext represents the message after encryption. The encryption key is used to encrypt the plaintext or decrypt the ciphertext, which is the same for XOR-based symmetric encryption and decryption. Fortunately, the encryption key can also be generated based on the intrinsic stochasticity of resistive switching in memristors,[39–41] which can be achieved using the same set of devices.

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In the present work, the encryption key was generated based on the cycle-to-cycle variation of HRS in unipolar memristors. Specifically, the resistance in the HRS of the device (R-HRS$_i$) is compared against that in the preceding cycle (R-HRS$_{i-1}$), $i \geq 1$. The ith bit of the encryption key is defined as "1" when R-HRS$_i$ − R-HRS$_{i-1} \geq 0$, and vice versa. Figure 5e–j presents experimental results from a memristor array fulfilling encryption and decryption of the ASCII codes of 3 capital letters "P", "K", and "U", namely, "01010000", "01001011", and "01010101", using an encryption key "00000111" representing "BEL" that is generated from hardware using the abovementioned approach. One can see from Figure 5e–g that correct results of "$01010000_{(P)}$ XOR $00000111_{(BEL)}$ = $01010111_{(W)}$", "$01001011_{(K)}$ XOR $00000111_{(BEL)}$ = $01001100_{(L)}$", and "$01010101_{(U)}$ XOR $00000111_{(BEL)}$ = $01010010_{(R)}$" were obtained, leading to ciphertext of "W", "L", and "R" that is stored in the array. Figure 5h–j further shows experimental results from the decryption process, where the correct results of "$01010111_{(W)}$ XOR $00000111_{(BEL)}$ = $01010000_{(P)}$", "$01001100_{(L)}$ XOR $00000111_{(BEL)}$ = $01001011_{(K)}$", and "$01010010_{(R)}$ XOR $00000111_{(BEL)}$ = $01010101_{(U)}$" were obtained once again, leading to the successfully recovered plaintext of "P", "K", and "U". Such hardware encryption and decryption based on memristor logics and intrinsic stochasticity has a great potential in hardware security.

6. Efficient Implementation of 1-Bit Binary Full Adder

Lastly, we experimentally demonstrate that 1-bit binary full adder can be built based on only 5 unipolar devices and can give the correct calculation results in 8 logic cycles. For 1-bit binary full adder, there are three inputs (addend A, summand B, and carry-in C_i) and two outputs (summary S and carry-out C_o), and the output results can be written as

$$S = A \oplus B \oplus C_i \tag{8}$$

$$C_O = \overline{\overline{(A \oplus B) \cdot C_i} \cdot \overline{A \cdot B}} \tag{9}$$

Figure 6a lists the corresponding logic sequence, and the operation details in the 2 × 3 memristive array are illustrated in Figure S5 in the Supporting Information. First, all the 5 devices are initialized to HRS by applying $V_{op,r}$ to all the WLs and "Ground" to both BLs (step 1), followed by the sequential logic operations (steps 2–8). During the entire logic process, the definition of input logic variable "1" keeps unchanged given that both XOR and NAND define the voltage level $V_{op,s}$ as input "1", thus decreasing the complexity for signal control. It is worthwhile pointing out that signal conversion needs to be performed in steps 3 and 6 due to the nonstateful nature of the logic (Figure 6a), where the resistance state needs to be read out and converted to voltage signals, serving as logic inputs in the next step. Figure 6b shows the experimental results of the 1-bit binary full adder for all the possible inputs, where correct results have been successfully obtained. The present implementation using 5 devices and 8 logic cycles compare favorably with existing memristor logic approaches in terms of area and latency,[13,15,16] once again showing the high efficiency of unipolar memristor-based logic.

7. Conclusion

In summary, here we have proposed and experimentally demonstrated an efficient in-memory logic approach based on memristors, which is capable of implementing all 16 Boolean logic functions in the same cell in less than 3 logic steps. The unipolar memristors in this work were optimized via confinement of filament diameter and thus the switching location, by introduction of a $Ta_2O_5/SiO_2/Ta_2O_5$ trilayer as the switching medium, which has effectively improved the operation speed and switching uniformity. A novel hardware encryption system is further demonstrated based on the unipolar memristors, where both the encryption and decryption processes were performed by the memristor-based XOR logic and the encryption key was generated from the intrinsic stochasticity of resistive switching effects. Other computation tasks including the calculation of Hamming distance and 1-bit binary full adder have also been achieved. The high efficiency of the memristor logic shown at both the cell level and the array level in this study could be of significance for future development of non-von Neumann computing architectures.

8. Experimental Section

Device Fabrication: The $Pd/Ta_2O_5/Pd$ unipolar devices were fabricated on SiO_2/Si substrates using the following process. First, 5 nm Ti as the adhesion layer and 30 nm Pd as the bottom electrodes were consecutively deposited by electron beam evaporation. Then, 13 nm Ta_2O_5 as the switching layer was deposited by RF-sputtering using a Ta_2O_5 target in Ar atmosphere at room temperature. Subsequently, 40 nm Pd was deposited as the top electrodes by electron beam evaporation. Finally, the bottom electrodes were exposed by dry etching technique for electrical measurements. The bottom electrodes and the top electrodes were patterned using photolithography process followed by film deposition and lift-off processes. In the $TiN/Ta_2O_5/SiO_2/Ta_2O_5/TiN$ devices, 10 nm Ta_2O_5/3 nm SiO_2/10 nm Ta_2O_5 as the switching layers were successively deposited by RF-sputtering at room temperature without breaking the vacuum. 30 nm Pd/10 nm TiN was adopted as the bottom electrode and 10 nm TiN/30 nm Pd was used as the top electrode. Both crossbar arrays and single devices were fabricated in this work. The size of devices in the crossbar array was 2 × 2 μm^2, and the single devices with a common bottom electrode had a size of 50 × 50 μm^2.

Electrical Measurements: All the electrical measurements on the Ta_2O_5-based unipolar memristors, including both DC sweep and pulse operations, were performed in ambient environment using Agilent B1500A semiconductor parameter analyzer and a Signatone probe station.

Microstructural Characterization: The TEM samples in this work were prepared by focused ion beam (FIB) technique using a dual-beam FIB system (FEI Helios Nanolab workstation). During FIB patterning, the sample was first coated by a Pt layer deposited using the electron beam to avoid surface damages, followed by higher-rate Pt coating using normal ion beam process that served as the majority of the protective layer during FIB cutting. In the end of the sample thinning, low energy Ga^+ ion milling with care was used to obtain high-quality and thin TEM specimens. The specimens were then subjected to TEM, STEM, and EDS characterizations (FEI Talos). The EDS measurements were performed in the STEM mode to obtain high spatial resolution.

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(a)

Operating sequence	Step	Device	WL_1	WL_2	WL_3	BL_1	BL_2
Initialization	1		Vop,r	Vop,r	Vop,r	Ground	Ground
$A \oplus B$	2		A	/	/	B	/
Signal conversion $A \oplus B$	3		Vread	/	/	Ground	/
$A \oplus B \oplus C_i$ (S)	4		/	$A \oplus B$	/	C_i	/
$\overline{A \cdot B}, \overline{(A \oplus B) \cdot C_i}$	4		A	$A \oplus B$	/	/	Vop,s
	5		B	C_i	/	/	Vop,s
Signal conversion $\overline{A \cdot B}, \overline{(A \oplus B) \cdot C_i}$	6		Ground	Ground	/	/	Vread
$\overline{\overline{(A \oplus B) \cdot C_i} \cdot \overline{A \cdot B}}$ (C_o)	7		/	/	$\overline{(A \oplus B) \cdot C_i}$	Vop,s	/
	8		/	/	$\overline{A \cdot B}$	Vop,s	/

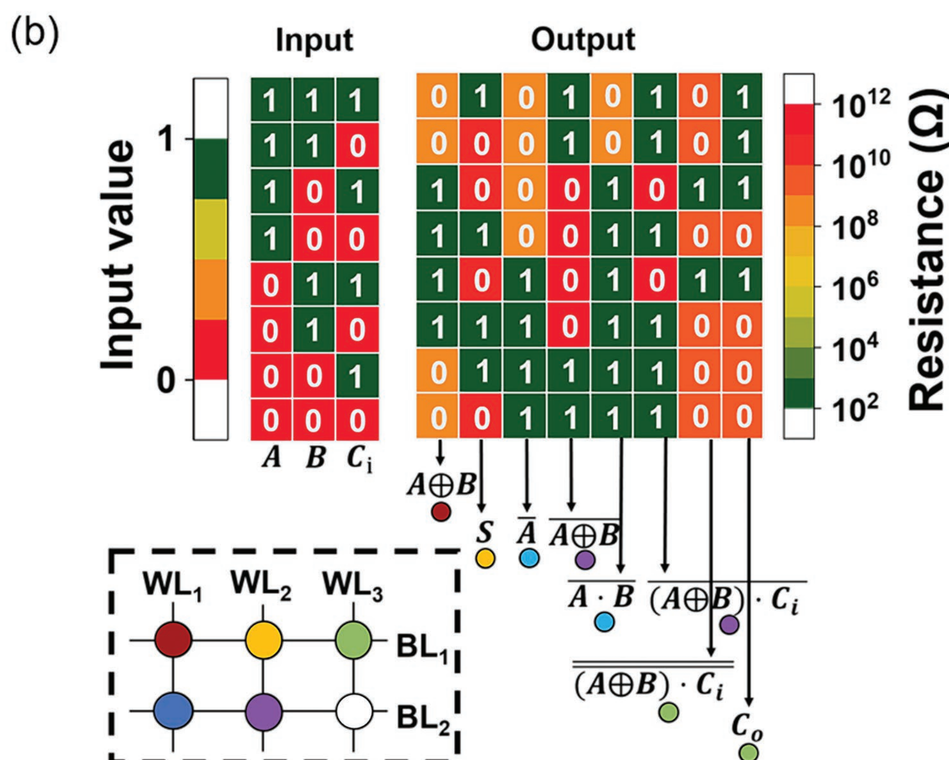

Figure 6. 1-bit binary full adder based on XOR and NAND logic in 2 × 3 unipolar memristive array. a) The operating sequence of the 1-bit binary full adder. The five devices are indicated by different colors. The voltage signal "$V_{op,s}$" represents input "1" during the entire logic process. Here, the symbol "/" in write steps represents protecting voltage to prevent write disturb and the symbol "/" in read steps represents floating terminals without electrical signals. b) Experimental logic results for different logic inputs. The corresponding logic function of each output column is drawn by arrows and labeled. Logic functions labeled on the same horizontal line can be executed in the same step.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

Boolean logic, encryption, full adder, Hamming distance, in-memory computing, memristors

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