Efficient Region-aware P/G TSV Planning for 3D ICs

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***Abstract*—Power delivery network (PDN) design is one of the most critical challenges in 3D Integrated Circuits (IC) design. In existing studies, to ensure the robustness of the 3D PDN, the number of TSVs was always increased inefficiently to mitigate the IR-drop and power noise. However, the overhead for connections is a crucial obstacle to the development of 3D ICs. Consequently, an efficient TSV topology is needed to reduce the overhead of TSVs while meeting the power supply requirements. The redundant TSVs may introduce more keep-out zones, decrease the core utilization of the chip, and lead to high cost. In this paper, we propose a region-aware TSV planning algorithm which can distribute TSV resources non-evenly over different areas according to their IR-drop constraints separately. This method can use fewer power TSVs to meet the power integrity constraint of the whole chip while guaranteeing the functionality. Furthermore, to ensure the practicability, we also take the whitespace into account. Experimental results show that, the proposed algorithm can save on average 42% and 27% power TSV resources without and with whitespace consideration respectively compared with the evenly TSV planning algorithm.**

***Index Terms*—3D power delivery network, region-aware TSV planning, non-evenly TSV topology, distributed IR-drop constraint, whitespace consideration**

I. Introduction

With continued technology scaling, traditional integrated circuit design methodologies face some severe challenges, such as large interconnect delay and high leakage power. In recent years, 3D ICs have been proposed as a promising solution to cope with these challenges and continue the Moore's Law. For a 3D chip, multiple dies are stacked together with vertical interconnects such as the through-silicon-via (TSV) [1]. 3D integration technologies show significant advantages including considerable wire length reduction on global interconnect; smaller footprint due to the increasing cell density; relaxed power, performance, and computational tradeoffs; and the possibility of heterogeneous integration of mixed-technology chips [2], [3].

Power delivery network (PDN) design is considered as one of the most critical challenges in 3D IC design. Even in the packages of today's industrial designs, more than half of the I/O pins (or C4 bumps) are dedicated to power and ground connections [4]. As multiple dies are stacked together into a smaller footprint, delivering current to all parts of the 3D stack while meeting the power supply constraints and the limitation of available TSVs becomes highly challenging [5].

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An unreliable chip design may lead to a severe IR-drop problem. The reduced supply voltage levels in the grid can increase the gate delay and harm the functionality of circuits, leading to timing violations, incomplete functionality and even silicon failures [6]. For example, 5% IR-drop may result in 15% or more performance degradation nowadays [7], [8]. Besides, the IR-drop on the terminal circuits should always be limited within 10% of the supply voltage [9].

Numerous studies spring up these years in the field of 3D power delivery network design. However, most studies tended to increase the number of TSVs to mitigate problems such as IR-drop. Besides, most studies employed the uniform IR-drop constraint on each layer of one chip while some still adopted the evenly TSV topology which may introduce a great deal of redundant TSVs. In this work, we proposed an efficient region-aware TSV planning algorithm. In consideration of that different functional areas may have different tolerable IR-drop thresholds in a real chip, the algorithm can distribute TSV resources over different areas according to their IR-drop constraints separately. This method can use fewer power TSVs to meet the power integrity constraint of the whole chip and save the cost. To further enhance the practicability of the algorithm, we also take the whitespace into account. Considering the large size of a TSV and its related keep-out zone, TSVs can only be inserted in the whitespace between modules.

Our main contributions are listed as follows.

1) We investigate the IR-drop problem for TSV based 3D IC more precisely with subdivision and formulate the regional distributed IR-drop constraint problem.
2) We propose the region-aware TSV planning algorithm to tackle the regional distributed IR-drop constraint problem with a non-evenly TSV topology. Furthermore, to enhance the practicability, we also take the whitespace into account when planning P/G TSVs. In comparison with the evenly TSV planning algorithm, our method can save on average 42% and 27% TSV resources without and with whitespace consideration.

The rest of the paper is organized as follows. Section II presents our motivation and overviews the related work. Section III formulates the region-aware TSV planning problem and Section IV describes the details of our algorithm. Experimental results are shown in Section V. Finally we conclude the paper in Section VI.

II. Motivation and related work

A. Related Work

In the last few years, fruitful researches have explored 3D power delivery network design and TSV planning.

Most of related works employed the distributed TSV topology. A 3D IC floorplan and P/G network co-synthesis tool was proposed by Falkenstern *et al* [10]. During the co-synthesis process, they tried to minimize the IR-drop and the routing area of the P/G wires at the same time. 2D meshes for each tier could have different pitches in order to balance P/G area and IR-drops in their work; but the TSVs were evenly distributed for each layer. Healy *et al* investigated the influence of different TSV topologies and concluded that an evenly distributed TSV topology was better to mitigate the IR-drop and the power noise [11]. They also concluded that the IR-drop problem could be efficiently alleviated by increasing the density of TSVs. A comprehensive research was done by Khan *et al* [12]. They compared the results of average IR-drops generated by several methods including increasing the TSV density and verified that increasing the TSV density is a suitable approach to reduce the average IR-drop. They also investigated the influence of different TSV topology. Yu *et al* proposed a simultaneous power delivery and thermal integrity optimization method to reduce the number of non-signal TSVs [13]. They also employed an evenly distributed TSV topology and verified that the increase of TSV density can decrease the power noise.

Several studies considering the non-evenly TSV distribution topology were proposed. Li *et al* took the sensitivity of resistance into account and proposed a non-evenly thermal-aware TSV planning algorithm in order to minimize the IR-drop on the entire chip [14]. They verified the efficiency of their method on floorplan-generated benchmarks. Jung *et al* proposed another non-evenly TSV planning algorithm [15]. They extracted a simple model from a real physical design, found the worst IR-drop regions and inserted P/G TSV in that area iteratively until the worst IR-drop met the threshold. Shuai *et al* analyzed the effects of several P/G TSV topologies on P/G noise including cross distribution and evenly distribution TSV topologies [16]. They found that the cross P/G TSV topology had the best performance in reducing the P/G noise.

All the methods mentioned and also most of existing researches did not consider the whitespace which caused the lack of practicability. Zhong *et al* pointed out that the TSV assignment came under the influence of the whitespace distribution in a given 3D floorplan and proposed an algorithm called whitespace insertion (WSI) to make the whitespace distribution in the given floorplan more reasonable for TSV insertion [17]. Li *et al* proposed a whitespace-aware 3D-MMM algorithm for 3D clock tree topology generation [18]. They bounded the clock TSVs in the whitespace blocks without overlap. The awareness of whitespace has a profound effect on researchers of this area.

B. Our motivation

The researches related to IR-drop problem can be roughly divided into two categories: The first category concentrates on TSV planning to meet the uniform IR-drop constraint on the whole chip, and the second category focus on minimizing the IR-drop using limited TSV resources.

The reliability of power delivery network is crucial. A quantitative exploration should be employed rather than minimization of IR-drop. The existing works considering definite IR-drop constraints all postulated that they are identical on one tier. If the IR-drop constraints are identical, they must meet the most strict constraint. For instance, if there are two IR-drop constraints 3% and 5% over different parts of the chip, the uniform IR-drop constraint should be 3% in order to provide protection for the entire chip. The overprotection for area with loose IR-drop constraint may cause the waste of TSV resources. Considering that TSV fabrication causes tensile stress around TSVs and results in significant carrier mobility variation in the devices near TSVs, additional keep-out zone (KOZ) is adopted to prevent any devices/cells from being impacted. Owing to the large TSV size, large amount KOZ can significantly reduce the placement area available for cells and result in a high cost [19], [20]. The overhead for connections is a crucial obstacle to the development of 3D ICs. To reserve more TSV resources and reduce the overhead of TSV area, the number of power TSVs should be minimized while the IR-drop constraints are met and the functionality is complete. Therefore, we propose the region-aware method to tackle this problem which can use TSVs more efficiently with a distributed IR-drop constraint and a non-evenly TSV topology.

Additionally, in the most commonly used face-to-back (F2B) bonding technology, TSVs must tunnel through the substrate of one tier [21]. Under the current technology, TSVs are usually much larger than the vias in the metal layers, so they should be placed in the whitespace between the modules in the device layer. To enhance the practicability, the planning algorithm must be whitespace-aware. Consequently, we also take the whitespace into account.

III. Problem formulation

A. Modeling of 3D Power Delivery Network

An example of a 3D power delivery network adopted in this paper with 4 tiers using the flip-flop package technology [22] is shown in Figure 1. The power delivery network consists of three components: the P/G networks on each tier, P/G TSVs, and the power pads (C4 bump). The P/G network on each tier is the same as 2D chips and considered as a $N \times N$ P/G mesh.

The TSV model we adopt is shown in Figure 2 [23]. R_t and C_t represent the parasitic resistance and capacitance of one P/G TSV respectively.

In static analysis, only resistance is considered in the circuit model. Thus, the P/G network is modeled as resistors and current sources, a TSV is modeled as a resistor, and a power

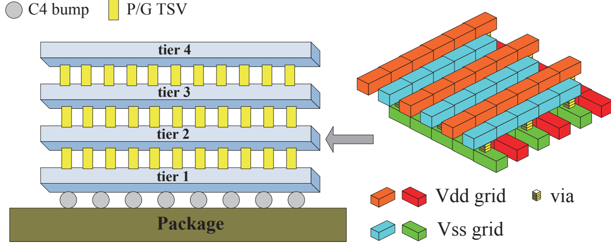

Fig. 1. 3D power delivery network

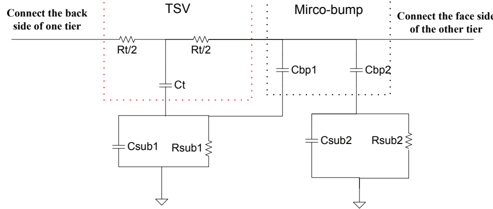

Fig. 2. Model of the TSV

pad is modeled as a resistor connected to a ideal voltage source.

The on-chip parameters and characteristics of the benchmarks used in experiments are adopted and calculated through PTM(Predictive Technology Model) [24].

B. Problem description

The region-aware TSV planning problem for 3D power delivery network design can be formulated as following: Given the P/G network, the static IR-drop constraints of the functional areas on each tier, and the limitation of available power TSVs, generate a suitable TSV distribution topology and output the TSV location information and a static voltage distribution map.

A simple example is shown in Figure 3. Each tier of the 3D chip can be divided into several blocks according to the input. The IR-drop constraint can be concluded as: for every node of the power delivery network, its corresponding voltage V must satisfies

$$V \geq (1 - k_i)V_{DD} \quad (1)$$

when this node is in block i. The coefficient k_i is the max allowed ratio of IR-drop in block i such as 4%. This constraint can ensure that this area of the chip has enough power to function correctly and reach an acceptable performance.

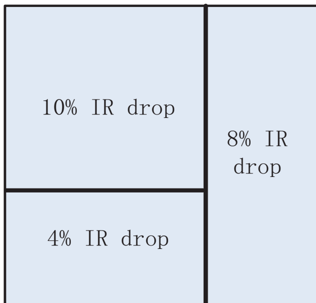

Fig. 3. A simple example for different IR-drop areas on one tier

C. Whitespace consideration

In 3D ICs, the vertical bonding technology can be classified into three categories: face-to-face (F2F), back-to-back (B2B), face-to-back (F2B) [21]. In this paper, we adopt the F2B bonding. As shown in Figure 4, the vertical interconnect connects the back side of the upper tier and the face side of the other tier by tunneling through the substrate of the upper tier. Therefore, to ensure manufacturability of the chip, the TSVs must be restricted to the whitespace between macro modules.

In region-aware TSV planning with whitespace consideration, we input the positions of macro modules. The current sources are only generated in the modules. During the planning process, a TSV can only be inserted at a node out of modules.

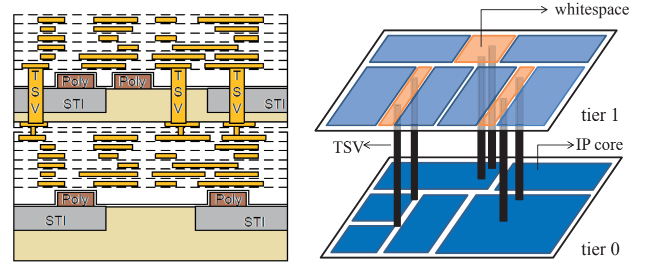

Fig. 4. In F2B bonding, TSVs can only be inserted in the whitespace of the upper tier

IV. Region-aware TSV planning algorithm

In this section, we first introduce the evenly distributed TSV planning algorithm which is regarded as the baseline to measure the effectiveness of our algorithm. After that, the region-aware TSV planning algorithm is explained in details. Next, we illustrate the impact of the parameter *AffectArea* and explain how to decide it.

A. Evenly distributed TSV planning algorithm

The flowchart of the evenly distributed TSV planning algorithm under a uniform IR-drop constraint is shown in Figure 5. In this case, only one IR-drop constraint V_{ir} is considered on the whole chip. According to the input information, an initial evenly distributed TSV topology is generated. In every iteration, we run the static analysis and check the validity. If not all nodes meet the uniform IR-drop constraint, we reduce the space between TSVs gradually until the uniform IR-drop constraint V_{ir} is satisfied everywhere or exiting with no solution because the TSV number constraint is violated.

B. Region-aware TSV planning algorithm

The region-aware TSV planning algorithm without whitespace consideration is shown in Figure 6. $IR\text{-}drop[i]$ is the IR-drop constraint at node i according to the input. We assume that $V[i]$ is the voltage at node i and *AffectArea* is the area that one TSV can affect.

The flow of the algorithm is explained below:

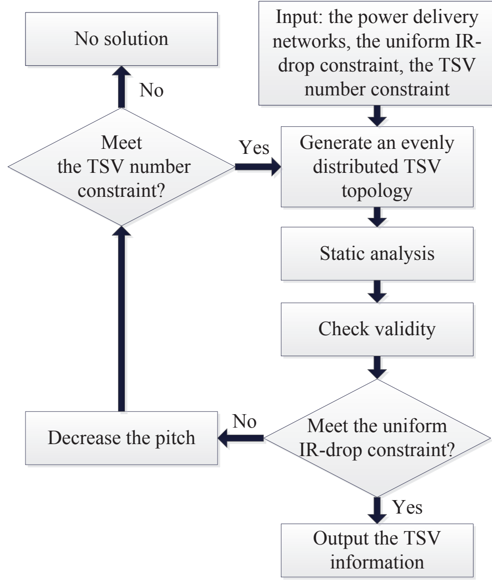

Fig. 5. The evenly distributed TSV planning algorithm

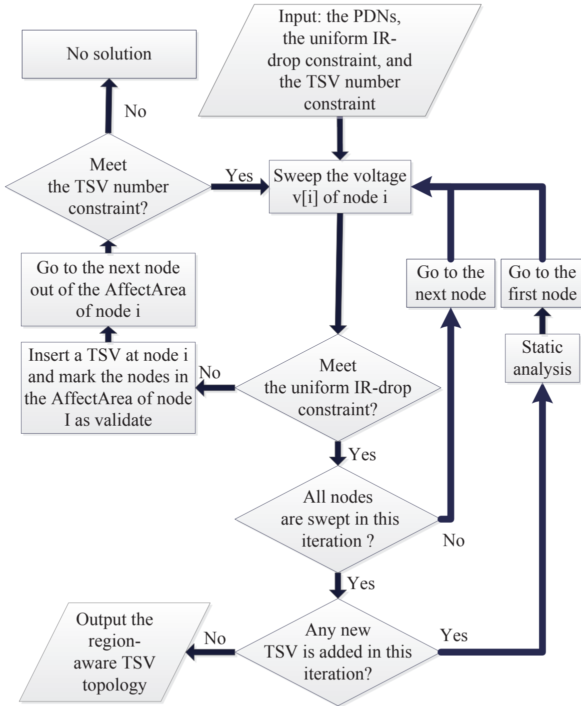

Fig. 6. The region-aware TSV planning algorithm

1) Let the uniform IR-drop constraint V_{ir} of the evenly distributed TSV planning algorithm be the most loose IR-drop constraint above all input constraints among all blocks:

$$V_{ir} \;=\; Max(IR-drop[i]),\ \forall\ i. \tag{2}$$

We generate the initial TSV topology with the evenly planning algorithm.

2) Sweep the voltage of each node and check whether it meets the $IR-drop[i]$ constraint.
   a) If the constraint of the current node is satisfied, then sweep the next node.
   b) If the constraint is not satisfied, insert a power TSV at this node and check the total number of TSVs. If the number of TSVs at present doesn't exceed the allowed maximum number, mark all the nodes in the *AffectArea* of the TSV as valid and sweep the next node.
3) When all the nodes are swept in this iteration, check whether there is any new power TSV inserted in 2).
   a) If some new power TSVs are inserted during the latest iteration, then simulate the whole power delivery network again and goto 2).
   b) If not, then we can conclude that the present TSV topology can satisfy all the IR-drop constraints and output the result.

Considering the fact that TSVs can only be inserted into whitespace, we introduce an additional adjustment into our algorithm: We first input the positions of the macro modules and mark all nodes in whitespace. The floorplan does not change during the planning process, so the distribution of whitespace remains the same. When planning TSVs, if the location to insert a TSV is in one module, we adjust it to the nearest whitespace.

In our algorithm, we use a direct method to determine the node to insert TSV: We sweep all the nodes, if the IR-drop constraint at this node is not met, we insert a TSV here. This method brings a great benefit that we can insert numerous TSVs during one iteration and reduce the number of iterations. Because one iteration requires a static analysis and usually causes quite a few time consumption, the reduction of iteration can accelerate the planning greatly.

C. Discussion of "AffectArea"

In 2D flip-chips, as packages consist of almost ideal current sources distributed frequently and uniformly above the chip, the supply voltage is generally lowered from the C4 bump. In 3D PDNs, TSVs play the role of C4 bumps. Considering this fact, a TSV can only affect the area in its neighborhood and ensure the supply voltage. To reduce the number of iterations and accelerate the TSV planning process, we need to insert necessary TSVs as many as possible during one iteration. To achieve this goal, we define the area that one TSV can affect as the parameter *AffectArea*. When one TSV is inserted, the nodes in its *AffectArea* are marked as valid and we can continue inserting TSVs in other areas during this iteration.

To achieve the best performance of the region-aware planning algorithm, a reasonable parameter *AffectArea* should be chosen following the equation beneath:

$$AffectArea = \frac{I_{TSV}}{\alpha \cdot \frac{P}{V_{DD}}} \tag{3}$$

where I_{TSV} is current load capacity of one TSV, P is the average power consumption per unit area, V_{DD} is the supply voltage, and α is parameter related to the wire size and the clearance between wires. $\frac{\alpha \cdot P}{V_{DD}}$ represents the average number

of nodes that a power node connects to. We can calculate I_{TSV} based the current load capacity of copper wire and the size of power TSV.

If *AffectArea* is too small, a degradation of the algorithm may occur: To meet the IR-drop constraints, more TSVs are needed. This is because if *AffectArea* is smaller than the area that a TSV can guarantee, in the planning process, more TSVs will be inserted and their affected areas are overlapped. On the contrary, if *AffectArea* is too large, the number of iterations will increase. This is because only a few TSVs will be inserted during one iteration, which cannot meet the IR-drop constraints on the whole chip. The time consumption and the complexity of the algorithm will both increase.

V. Experimental results

In this section, "evenly planning" means that the result is generated by the evenly TSV planning algorithm. We regard it as a baseline to evaluate the effectiveness of our algorithm. First, we implement our algorithm on a simple benchmark to verify its performance. Next, two benchmarks generated from the results of 3D floorplan are tested. After that, we use some benchmarks to simulate some industrial benchmarks and verify the performance of the whitespace-aware method. The influence of the selection of *"AffectArea"* is discussed in the end. It should be pointed out that the IR-drop constraints in the experiments are not based on any specific design but simply selected as a case study following a basic guideline that the IR-drop should always be limited within 10% [9]. The parameters are user dependent. We also had implemented this algorithm to help chip designers locate the P/G TSVs in a 3D SAR ADC [25].

The region-aware TSV planning software is implemented using C++ language. The simulation tool we choose is H-S3DPG [26]. All experiments are performed on a PC with an Intel CORE i7-3610QM CPU @2.30 GHZ(4 cores) and 8 GB RAM.

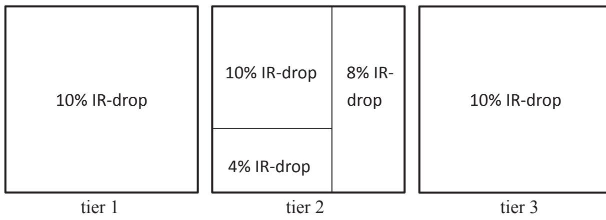

Fig. 7. The IR-drop constraints of tiers

A. Verification of the region-aware TSV planning algorithm

The parameters of the power delivery network benchmark are shown in Table I. As mentioned in Section III, the characteristics of the wire and TSV are calculated using the PTM model [24] and the model in [23] respectively. The benchmark is a three-tier 3D power delivery network. The number of nodes in each tier is 10000. The chip is a flip-flop chip [22], the bottommost tier connects the package through power pads. There are 10×10 power pads evenly distributed on the bottommost tier.

TABLE I
PARAMETERS OF THE BENCHMARK

Parameter	Value
Number of tiers	3
Number of nodes on one tier	10000
Number of power pads	100
Supply voltage	0.8V
Average current density	$128A/cm^2$
Width of wire	2.5 μ m
Clearance between two wires	10 μ m
Thickness of wire	0.14 μ m
Diameter of P/G TSV	10 μ m
Resistance of TSV	0.083 Ω

The distribution of IR-drop constraints is shown in Figure 7. On tier 1 and tier 3, the IR-drop constraint is 10% V_{DD}. Particularly, on tier 2, there are some functional modules which are sensitive to the supply voltage, so there are three kinds of IR-drop constraints: 10% V_{DD}, 8% V_{DD} and 4% V_{DD}.

In evenly TSV planning, the density of TSVs is high to ensure that the supply voltage for the area with strictest IR-drop constraint. Meanwhile, in the region-aware TSV planning, the TSV topology can be adjusted to the distribution of IR-drop constraints. Only necessary TSVs will be inserted. The total number of TSVs in evenly and region-aware case are shown in Table II.

TABLE II
COMPARISON OF TSV CONSUMPTION

Algorithm	The total number of power TSVs
Evenly planning	162
Region-aware planning	84
Reduction of TSVs	48 %

The result shows, in consideration of the different tolerable IR-drop thresholds of different function modules, the region-aware TSV planning algorithm can save about 48% power TSVs in comparison with the evenly TSV planning algorithm. To confirm that the TSV topology generated by our algorithm is valid, we also draw the full static voltage distribution map in Figure 8 and Figure 9.

From the comparison between Figure 8 and Figure 9, we can find that:

1) The evenly planning algorithm provides overprotection to some area of the chip. The region-aware algorithm inserts more TSVs in the "4% IR-drop" area than the area of loose IR-drop constraints to provide protection for areas separately according to their IR-drop constraints.

2) The static voltage map of region-aware TSV planning is similar to the assumption in Figure 7; and in Figure 8, we cannot distinguish the difference between different areas. The IR-drop constraints in both case are not violated.

Using the region-aware TSV planning algorithm, we can utilize the limited TSV sources more effectively while satisfying the demands of supply voltage. In 3D IC technology, the power TSV is bigger than clock TSV and signal TSV because of the much bigger current load. Thus, the number of power TSVs, the wire resource, and the space source can be saved using our region-aware TSV planning algorithm.

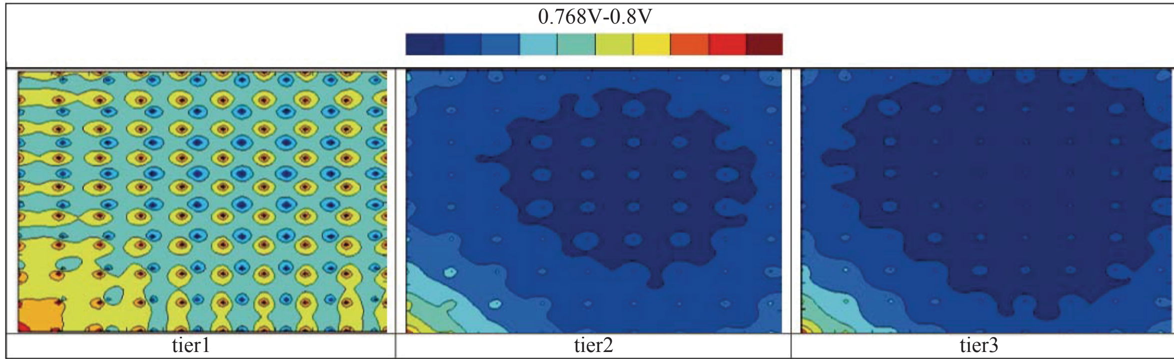

Fig. 8. The voltage map of evenly TSV planning

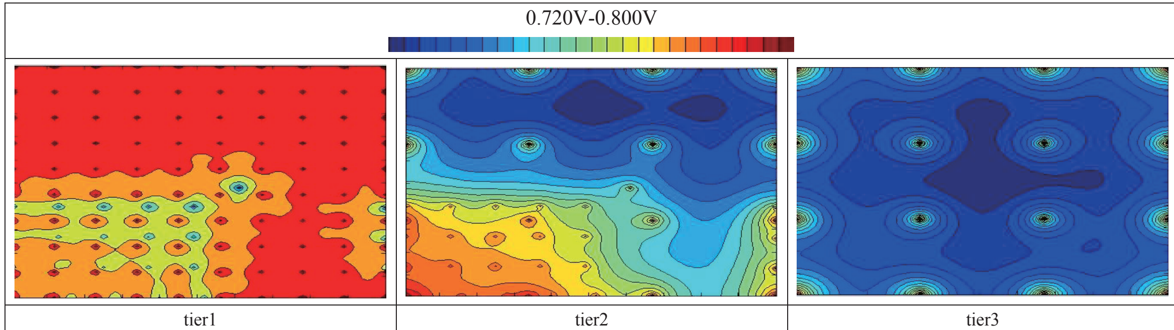

Fig. 9. The voltage map of region-aware TSV planning

B. Results of floorplan-generated benchmarks

We generate the P/G networks with the parameters introduced in Subsection A for 3D floorplan benchmarks [14]. The size, connection and delay information of each module is provided in the benchmarks. We implement the results of floorplan on our P/G network and partition the power grid into several blocks. In the test of benchmark *ami33*, the IR-drop constraints of the modules on and off the critical path are set to be 5% and 8% respectively. The IR-drop constraint for whitespace is 10%. As for *ami49*, the corresponding IR-drop constraints are: 6%, 8% and 10%. The results are shown in Table III. With these two benchmarks, our algorithm can achieve 37.7% and 39.5% TSV reduction respectively.

TABLE III
RESULTS OF FLOORPLAN-GENERATED BENCHMARKS

Benchmark	Tiers	Size	AffectArea	TSV(region-aware)	TSV(evenly)
ami33	4	100 × 100	12	187	300
ami49	4	105 × 105	12	147	243

C. Performance with whitespace consideration

To verify the performance of our algorithm with whitespace consideration, we generate benchmarks to simulate the functional areas distribution in the benchmarks extracted from industrial designs [5]. An example is shown in Figure 10. The total number of P/G TSVs is only eight in the original benchmark, which is inconvenient for comparison, so we adjust the P/G wire parameters and the current density and generate the benchmark ourselves. The size of 3D-μp and 3D-TxRx are 4832μm $\times$ 4832μm and 1900μm $\times$ 1900μm, so the space length between P/G wires in these two P/G networks are 48.32 μm and 19 μm. The electrical parameter are also calculated through PTM model [24]. The IR-drop constraints are set according to the power consumption maps.

TABLE IV
RESULTS OF BENCHMARKS TO SIMULATE 3D-μP AND 3D-TXRX

Benchmark to simulate	Tiers	Size	AffectArea	TSV(region-aware)	TSV(evenly)
3D-μp	2	100 × 100	12	76	100
3D-TxRx	3	100 × 100	12	140	200

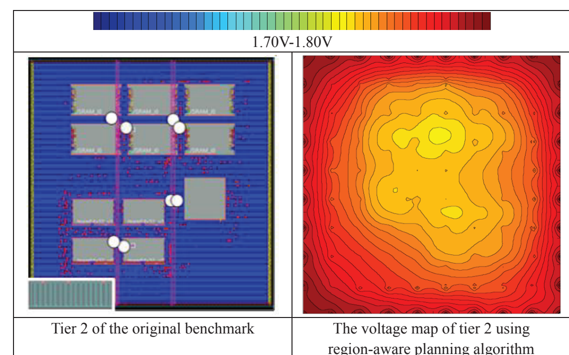

Fig. 12. Tier 2 of the original benchmark 3D-TxRx and its corresponding voltage map

The results are shown in Table IV. In the experiment of benchmark simulating 3D-μp, the proposed algorithm can achieve 24% TSV reduction. In another experiment, the TSV save ratio is 30%. We also draw the voltage maps of the benchmark simulating 3D-μp in Figure 11. Tier 2 of the original benchmark 3D-TxRx and its corresponding voltage is shown in Figure 12. In these two benchmarks, our algorithm

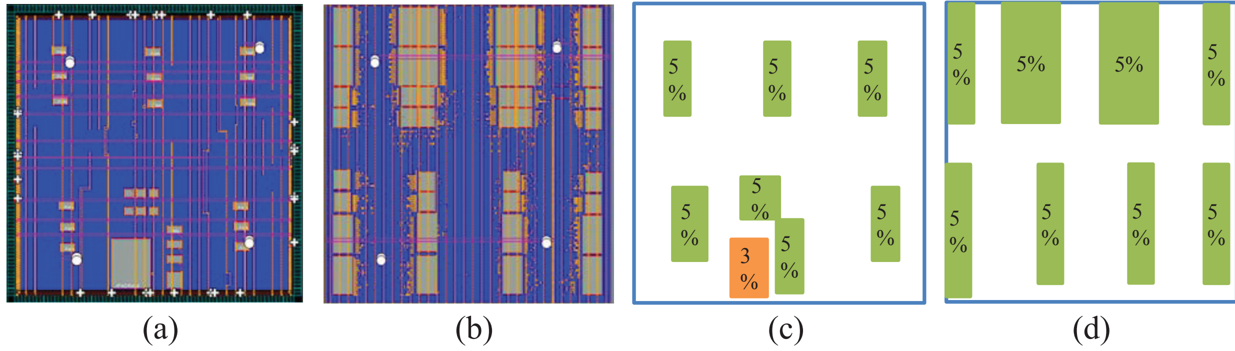

Fig. 10. Problem description with whitespace consideration: (a),(b) tier1 and tier 2 of benchmark 3D-μp [5]; (c),(d) the inputs for our algorithm to simulate the benchmark

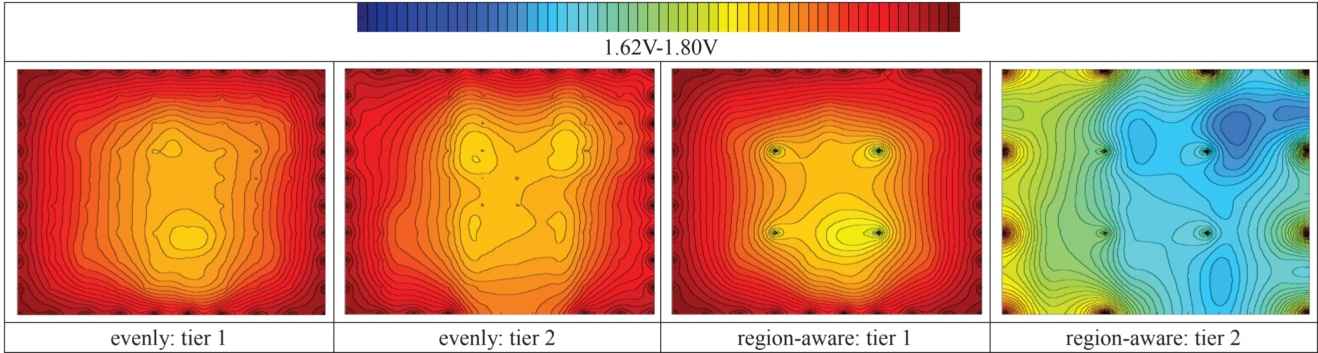

Fig. 11. The voltage maps of the benchmark simulating 3D-μp [5] with different TSV planning algorithms

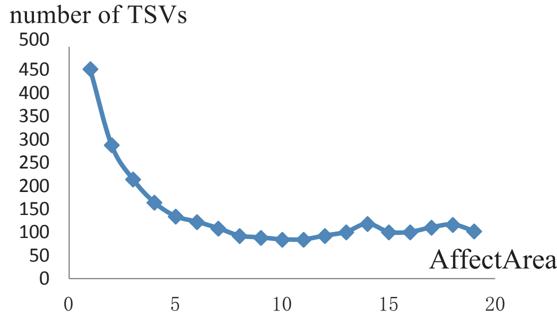

Fig. 13. The relation between *AffectArea* and the number of TSVs

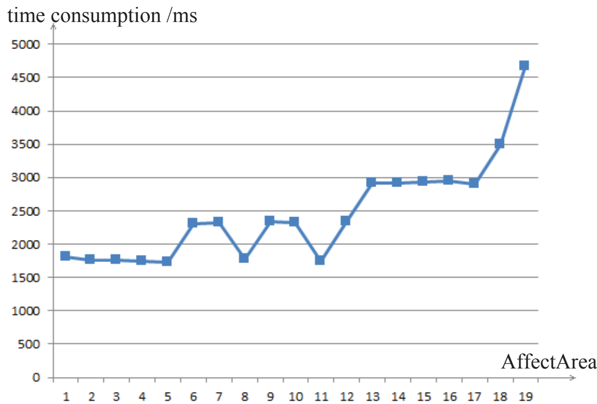

Fig. 14. The relation between *AffectArea* and time consumption

does not show great advantages. This is because current sources are only generated in the modules. Therefore, the IR-drop in other areas are small.

D. The influence of "AffectArea"

As shown in Figure 6, in the region-aware TSV planning algorithm, once a new power TSV is inserted at a node, we mark the nodes in the *AffectArea* around the TSV as valid. It's obvious that the selection of *AffectArea* has an impact on the performance of our algorithm. To evaluate the influence, we change the *AffectArea* from 1×1 nodes to 19×19 nodes to compare the results with different *AffectArea*. The results are shown in Figure 13 and Figure 14.

The experimental results verify our estimation in section IV.C. If *AffectArea* is smaller than the area that a TSV can actually guarantee, more TSVs will be inserted and the number of iteration decreases. Otherwise, if *AffectArea* is too large, the number of iterations will increase. This is because that only a few TSVs will be inserted during one iteration, which cannot meet the IR-drop constraints on the whole chip. The time consumption and the complexity of the algorithm will both increase.

In conclusion, a suitable *AffectArea* must be selected to accelerate the planning process while reducing the number of TSVs and the number of iterations. Users should calculate the parameter *AffectArea* follow equation (4) in order to let it be more approximative to the real area that one TSV can affect.

VI. Conclusion

The overhead for connections is a crucial obstacle to the development of 3D ICs. In this paper, we propose an efficient region-aware P/G TSV planning algorithm for 3D power delivery networks which involve a distributed IR-drop constraint, a non-evenly TSV topology, and the whitespace limitation. The non-evenly TSV topology combined with the distributed IR-drop constraint can prevent redundant TSVs. The whitespace limitation introduces the feasibility to apply this method in real designs. Combining these three considerations, the proposed method can save the overhead for vertical connections occupied by power TSVs while guaranteeing the power supply. The reduction of overhead for connections can increase the core utilization ratio, reduce the chip area, save the cost, and enhance the manufacturability of 3D ICs. Experimental results show that, the TSV topology generated by the proposed algorithm can ensure sufficient power supply for the whole 3D chip using 27% less power TSVs with whitespace limitation.

Considering the limits of this work, we would like to make improvements in the future including: Taking more constraints such as thermal and timing constraints into account. Using powerful methods like analytical method to avoid the initialization with evenly TSV topology. Embedding a more efficient method to decide the locations where TSVs insert during one iteration; For example, inserting TSVs at all the concave points in the voltage map. Implementing the proposed method to more specific designs and verifying its performance.

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