Wulong Liu

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Current Status

Ph.D. Candidate in Research Institute of Circuits and Systems Lab, Department of Electronic Engineering, Tsinghua University, China.
(Expected to graduate in Jul. 2015)

Education

2010.09 to present **Tsinghua University** **Beijing, R.P. China**
Ph.D. Candidate in Electronic Science and Technology
Advisor: *Prof. Huazhong Yang* (*Email: yanghz@tsinghua.edu.cn*)
Co-advisor:*Prof. Yu Wang* (*Email: yu-wang@mail.tsinghua.edu.cn*)

2012.10 to 2013.03 **Pennsylvania State University** **United States**
Visiting scholar in Computer Science and Engineering Department Supervised by *Prof. Yuan Xie* (*Email: yuanxie@cse.psu.edu*)

2006.09 to 2010.07 **Xidian Univeristy** **Xi'an, R.P. China**
B.S. in Integrated Circuit Design and Integrated System. Rank: 5/200

Internship Experience

2013.10 to present **AMD Research Lab** **Beijing, China**

- **Novel Chip-to-Chip Interconnect Exploration**: For the requirement of high-speed off-chip data communication, we explore the traditional electrical and novel optical-based chip-to-chip interconnect. We find that the novel optical-based interconnect can achieve higher data communication bandwidth with the given power budget.
- **Low Power Clock Network**: Clock network is one of the major contributors for on-chip power. In this work, we investigate the resonant clock as a potential solution to reduce the power consumption in clock network by recycling the energy with on-chip inductors. Closed-form expressions for the resonant clock mesh and analytically analysis are derived. The proposed Matlab-based simplified circuit model can achieve 10^5 speedup compared to SPICE-based simulation.

(***Published two journal papers and two conference papers, applied two US patents and one software copyright***)

2009.1 to 2009.3 **National ASIC Center** **Beijing, China**

- **Radiation Robust-aware Standard Cell Library Design**: Radiation is one of the major threat for the chip reliability in the space. This project is to re-design the robust-aware 90nm and 65nm standard cells, including the modification of the design checking rules, parasitic parameters extraction, and ring-based gate layout modification.

Research Topics

- **Heterogeneous Integration of Micro-systems**: 3D stacking provides a good solution to integrate multiple heterogeneous functional units onto one chip, such as analog, digital, RF, MEMS. In this work, we investigate the system architecture and design optimization of the 3D heterogeneous ICs. We explore the 3D integration of mixed-signal system. In addition, we propose several design optimization for the 3D clock network. We also propose a hybrid structure of on-chip power system supplied for the embedded system. The experiment demonstrates the hybrid structure can increase 5x times lifetime of the practical wireless sensor node.
- **Memory Scheduling for Distributed Storage System**: For the both on-chip many-core system and large server cluster, distributed data storage can contribute to reduce the storage risk and enhance the data access efficiency. In this work, by leveraging the data communication overhead and the balance of memory, we propose an efficient memory scheduling algorithm and optimize the reliability for the distributed storage system.

Honors and Rewards

- ♦**National Graduate Scholarship** *2014.10*
- ♦**MHI Scholarship** *2013.9*
- ♦**Excellent Student Leader of Tsinghua University** *2011.12*
- ♦**Outstanding Graduate of Xidian University** *2010.7*
- ♦**Three Times of the First-Class Academic Excellence Scholarship (5/120)** *2007-2010*
- ♦**The Top-Class Academic Excellence Scholarship (1/120)** *2006.12*

Publications

[J1] **Wulong Liu**, *et al.* "On-Chip Hybrid Power Supply System for Wireless Sensor Nodes", in ACM Journal on Emerging Technologies in Computing Systems (**JETC**), Volume 10, No. 3, 2014. (**IF=0.8**)

[J2] **Wulong Liu**, *et al.* "Exploration of Electrical and Novel Optical Chip-to-Chip Interconnects", accepted by IEEE Design & Test, 2014. (**IF=1.6**)

[J3] **Wulong Liu**, *et al.*"Whitespace-Aware TSV Arrangement in 3D Clock Tree Synthesis", accepted by IEEE Transactions on Very Large Scale Integration (**TVLSI**), 2014. (**IF=1.2**)

[C1] **Wulong Liu**, *et al.* "Design Methodologies for 3D Mixed Signal Integrated Circuits: a Practical 12-bit SAR ADC Design Case", in the IEEE/ACM Design Automation Conference, **DAC 2014**, San Francisco, USA. (***Oral Presentation***)

[C2] **Wulong Liu**, *et al.* "Design Methodologies for 3D Mixed Signal Integrated Circuits: a Practical 8-bit SAR ADC Design Case", in the Work in Progress Session of the IEEE/ACM Design Automation Conference, **DAC 2013**, Austin, USA. (***Poster Presentation***)

[C3] **Wulong Liu**, *et al.* "Whitespace-aware TSV arrangement in 3D clock tree synthesis", in the IEEE Computer Society Annual Symposium on VLSI, **ISVLSI 2013**, Natal, Brazil. (***Oral Presentation***)

[C4] **Wulong Liu**, *et al.* "TSV-aware topology generation for 3D Clock Tree Synthesis", in the IEEE International Symposium on Quality Electronic Design, **ISQED 2013**, Santa Clara, CA, USA. (***Oral Presentation***)

[C5] **Wulong Liu**, *et al.* "On-chip hybrid power supply system for wireless sensor nodes", in the IEEE/ACM Asia South Pacific Design Automation Conference, **ASP-DAC 2011**, Yokohama, Japan. (***Oral Presentation***)

[C6] **Wulong Liu**, *et al.*"Modeling and Optimization of Low Power Resonant Clock Mesh", accepted by IEEE/ACM Asia South Pacific Design Automation Conference, **ASP-DAC** 2015. (***Oral Presentation***)

Patent

[1]**Wulong Liu**, Haixiao Du, Yu Wang, Jinguo Quan, Huazhong Yang, "TSV-based 3D clock network topology generation method", 201210293231.7

Software Copyright

[1] **Wulong Liu**, Haixiao Du, Yu Wang, Jinguo Quan, Huazhong Yang, "3D clock tree synthesis tool", 2012SR100965.

Teaching Assistant

- ♦**Teaching assistant in the course: "C/Unix Programming"** *2012.2 to 2012.7*

Skills and Endorsement

- ♦**Programming Languages**
  C/Unix Programming, C++, Perl, Verilog HDL/VHDL, etc.
- ♦**IC Design Tools**
  Matlab, SPICE, Cadence design suit tools, Synopsys design suit tools, etc.