Tianhao Huang

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Department of Electronic Engineering, Tsinghua University, Beijing, China

Education

Tsinghua University **Haidian, Beijing**
B. Eng. Candidate, GPA Accumulative – 92.5/100, Ranking – 6/194 *Sep. 2014 – Jun. 2018 (expected)*

The University of Texas at Austin **Austin, TX**
Exchange Student in ECE department , GPA – 4.0/4.0 *Jan. 2017 – May. 2017*

Scholarship and Awards

- Scholarship for Academic Innovation, **Tsinghua University** 2017
- Excellent Undergraduate Visiting Student Scholarship, **China Scholarship Council** 2017
- National Endeavor Scholarship (twice) 2016 – 2017
- *Zheng Geru* Scholarship for Excellent Academic Performance , **Tsinghua University** 2015
- *First Prize* in National Physics Olympics for University Students (Non-Physics Major) 2015
- Scholarship for Freshmen, **Tsinghua University** 2014

Research Interests

- Architecture and programming support for parallelizing irregular applications
- Domain-specific FPGA accelerator design

Research Experience

Nanoscale Integrated Circuits and Systems Lab, Tsinghua University **Haidian, Beijing**
Undergraduate Member, ***Advisor: Yu Wang*** *Sep. 2016 – Now*

- *Efficient Large-scale Graph Processing Accelerators*
  - Proposed a hybrid memory hierarchy, **HyVE**, which combines DRAM and Resistive RAM to provide an energy-efficient memory subsystem for graph processing accelerators.
  - Developed a multi-FPGA solution for large-scale graph processing, **ForeGraph**, which is the first published multi-FPGA system capable of handling billion-edge-scale graph datasets.
  - Currently developing an optimized implementation of ForeGraph as the senior design project.
- *Architectural Exploration of Graph Processing Systems*
  - Conducted an extensive research into existing graph processing systems on CPU, FPGA and Processing-in-memory (PIM) platforms.
  - Developed a fast direct-execution simulator based on DynamoRIO for PIM architecture, with the purpose of exploring performance of various prefetcher organizations in the logic die.

Computer Architecture Lab, ECE Department, CMU **Pittsburgh, PA**
Summer Intern, ***Advisor: James Hoe*** *Jun. 2017 – Aug. 2017*

- *Parallelization of SAT Solvers*
  - Studied SAT problem and well-known heuristics; built a CDCL (Conflict-Driven Clause Learning)

solver for profiling purposes.
- Proposed a parallelization method for constraint propagation in SAT solvers by mapping it into a graph algorithm.
- Developed a parallelized SAT solver based on MiniSAT and Galois, a parallel programming framework for irregular applications.

Publications and Manuscripts

- Guohao Dai, **Tianhao Huang**, Yuze Chi, Jishen Zhao, Guangyu Sun, Yongpan Liu, Yu Wang, Yuan Xie, Huazhong Yang, GraphH: A Processing-in-Memory Architecture for Large-scale Graph Processing, **submitted** to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.
- **Tianhao Huang**, Guohao Dai, Yu Wang and Huazhong Yang, HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing, **accepted** for publication in *Design, Automation and Test in Europe Conference & Exhibition, DATE 2018*.
- Guohao Dai, **Tianhao Huang**, Yuze Chi, Ningyi Xu, Yu Wang and Huazhong Yang, ForeGraph: Exploring Large-scale Graph Processing on Multi-FPGA Architecture, **accepted** for publication in *2017 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2017)*.

Course Projects

- A RF wireless mouse controller for PC based on finger gestures. Course: **Embedded Systems Lab**
- A convolution acceleration engine for CNN based on Xilinx Zedboard SoC, achieving a 2 orders of magnitude speedup compared to an ARM Cortex-A9 implementation. Course: **Digital System Design**
- A 5-stage pipelined MIPS processor. Course: **Fundamental of Digital Logic and Processor Lab**

Technical Skills

Proficient: C/Unix programming, C++, Verilog, Java, Python
Familiar: Xilinx/Altera toolchains, PCB design, x86/MIPS Assembly, Linux Shell

English Proficiency

GRE	Verbal – 162/170, Quantitive – 170/170, Analytical Writing – 4.0/6.0
TOEFL iBT	105/120 (Reading 30, Listening 28, Speaking 23, Writing 24)