Guohao Dai

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Education

Department of E.E., Tsinghua University, Beijing, China Sep. 2014 – now

Ph.D candidate, supervised by Prof. Yu Wang (Email: yu-wang@mail.tsinghua.edu.cn)

Department of E.E. & C.S., University of California, Berkeley, USA Oct. 2017 – Jun. 2018

Visiting Scholar, supervised by Prof. John Wawrzynek (Email: johnw@eecs.berkeley.edu)

Department of E.E., Tsinghua University, Beijing, China Sep. 2010 – Jul. 2014

Bachelor (Recommended)

- **GPA**: 90.4/100, **rank**: 18/210
- **Honor of Excellent Graduation Thesis**, Tsinghua University, "Accelerating Large-scale Graph Exploration based on FPGAs"
- **Typical courses**: "Linear Algebra"(100), "Coding Theory"(100), "Stochastic Process"(99), "Logical Design of Digital System"(98), "Digital Signal Processing"(97), "Probability Theory"(95)

Research Topics

Large-scale graph processing

Large-scale graph processing is widely studied in many domains. Performance of large-scale graph processing systems is one of the key problems in big data analysis and machine learning.

- **CPU-based system design.** Graph processing on both single machine systems and distributed systems are both widely adopted in industry and academia. My single machine system, NXgraph [ICDE 16], can achieve 3.8x speedup compared with the state-of-the-art single-machine system (GridGraph [ATC15]) and 1.8x speedup with a 64-node cluster (PowerGraph [OSDI12]).
- **FPGA graph processing framework design.** FPGAs can provide fine-grained parallelism of data processing. I make use of this characteristic and developed FPGA-based graph processing framework FPGP [FPGA 16] and ForeGraph [FPGA 17], which achieved 1.41x$\sim$2.65x throughput improvements over previous graph processing designs ([FCCM17]).
- **Graph processing architecture design.** Design at the architecture level provides sufficient bandwidth for graph processing. I designed graph processing architecture [TCAD] based on the processing-in-memory technique, which achieves 2 orders of magnitude speedup over conventional CPU designs and 3x throughput compared with the previous design (Tesseract [ISCA15]).
- **Energy-efficient graph processing.** I designed heterogeneous memory hierarchy to reduce the energy consumption of loading data in graph processing. I also designed energy-efficient graph computing units using emerging devices [DATE 18], which achieved 114x energy efficiency improvement over CPU-DRAM architectures.

Heterogeneous computing in the cloud and distributed systems

FPGA-based cloud computing has provided a new approach for users to get computing resources. I studied the efficient on-line task scheduling method and achieves 1.39x speedup [FPT 14].

Awards and Honors

Best Paper Award, first author, *Asia and South Pacific Design Automation Conference* Jan. 2019
Best Paper Nomination, second author, *Design, Automation & Test in Europe* Mar. 2018
Scholarship of Future Scholar, Tsinghua University (Top 2 in Dept. of E.E.) Sep. 2014
Scholarship of Comprehensive Merit, Tsinghua University (four times) Nov. 2018, 2016, 2013, 2011
Scholarship of SMT, DEK International Jul. 2011
First Prize in Beijing College Physics Competition, Beijing Physical Society Dec. 2011
First Prize in China Physics Olympiads (Anhui Division), Anhui Physical Society Dec. 2009

Publications

[J1] **Guohao Dai**, Tianhao Huang, Yu Wang, Huazhong Yang, John Wawrzynek, "HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing", to appear in *IEEE Transactions on Computers* (**ToC**), 2019. (**CCF-A**).

[J2] **Guohao Dai**, Tianhao Huang, Yuze Chi, Jishen Zhao, Guangyu Sun, Yongpan Liu, Yu Wang, Yuan Xie, Huazhong Yang, "GraphH: A Processing-in-Memory Architecture for Large-scale Graph Processing", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (early access)* (**TCAD**), 2018. (**CCF-A**).

[C1] **Guohao Dai**, Tianhao Huang, Yu Wang, Huazhong Yang, John Wawrzynek, "GraphSAR: A Sparsity-Aware Processing-in-Memory Architecture for Large-scale Graph Processing on ReRAMs", to appear in *Asia and South Pacific Design Automation Conference* (**ASP-DAC**), 2019. (**Best Paper Award, CCF-C**)

[C2] **Guohao Dai**, Tianhao Huang, Yuze Chi, Ningyi Xu, Yu Wang, Huazhong Yang, "ForeGraph: Exploring Large-scale Graph Processing on Multi-FPGA Architecture", in *ACM International Symposium on FPGA* (**FPGA**), 2017, pp.217-226. (**CCF-B, accepted 311 papers from 2009 to 2018, 23 are with the first author from mainland China**).

[C3] **Guohao Dai**, Yuze Chi, Yu Wang, Huazhong Yang, "FPGP: Graph Processing Framework on FPGA", in *ACM International Symposium on FPGA* (**FPGA**), 2016, pp.105-110. (**CCF-B, accepted 311 papers from 2009 to 2018, 23 are with the first author from mainland China**).

[C4] **Guohao Dai**, Yi Shan, Fei Chen, Yu Zhang, Yu Wang, Kun Wang and Huazhong Yang, "Online Scheduling for FPGA Computation in the Cloud", in *International Conference on Field-Programmable Technology* (**FPT**), 2014, pp.330-333.

[C5] **Guohao Dai**, Tianhao Huang, Yu Wang, Huazhong Yang, John Wawrzynek, "NewGraph: Balanced Large-scale Graph Processing on FPGAs with Low Preprocessing Overheads", in *IEEE International Symposium on Field-Programmable Custom Computing Machines* (**FCCM**), 2018, pp. 208-208. (poster)

[C6] Gushu Li, **Guohao Dai**, Shuangchen Li, Yu Wang and Yuan Xie, "GraphIA: An In-situ Accelerator for Large-scale Graph Processing", in *International Symposium on Memory Systems* (**MEMSYS**), 2018.

[C7] Tianhao Huang, **Guohao Dai**, Yu Wang and Huazhong Yang, "HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing", in *Design, Automation & Test in Europe* (**DATE**), 2018, pp. 973-978. (**Best Paper Nomination, CCF-B**)

[C8] Yuze Chi, **Guohao Dai**, Yu Wang, Guangyu Sun, Guoliang Li, Huazhong Yang, "NXgraph: An Efficient Graph Processing System on a Single Machine", in *IEEE International Conference on Data Engineering* (**ICDE**), 2016, pp. 409-420. (**CCF-A**)

[C9] Yubin Li, Yuliang Sun, **Guohao Dai**, Qiang Xu, Yu Wang, Huazhong Yang, "Approximate Frequent Itemset Mining for Streaming Data on FPGA", in *International Conference on Field-Programmable Logic and Applications* (**FPL**), 2016, pp. 1-4.

[C10] Yubin Li, Yuliang Sun, **Guohao Dai**, Yuzhi Wang, Jiacai Ni, Yu Wang, Guoliang Li, Huazhong Yang, "A Self-aware Data Compression System on FPGA in Hadoop", in *International Conference on Field-Programmable Technology* (**FPT**), 2015, pp. 196-199.

[C11] Sitao Huang, **Guohao Dai**, Yuliang Sun, Zilong Wang, Yu Wang, Huazhong Yang, "DTW-Based Subsequence Similarity Search on AMD Heterogeneous Computing Platform", in *International Conference on High Performance Computing and Communications & IEEE International Conference on Embedded and Ubiquitous Computing* (**HPCCEUC**), 2013, pp. 1054-1063.

Presentations

Tokyo, Japan — Jan. 2019
- *GraphSAR: A Sparsity-Aware Processing-in-Memory Architecture for Large-scale Graph Processing on ReRAMs*

Alibaba Group, Beijing, China — Jul. 2018
- *Accelerating Large-scale Graph Processing on CPUs and FPGAs*

Huazhong University of Science and Technology, Wuhan, China — Jul. 2017
- *Large-scale Graph Processing on CPUs and FPGAs*

University of California at Santa Barbara, CA, USA — Feb. 2017
- *Large-scale Graph Processing on Multi-FPGA Architecture*

University of California at Santa Cruz, CA, USA — Feb. 2017
- *Large-scale Graph Processing on Multi-FPGA Architecture*

Monterey, CA, USA — Feb. 2017

- *ForeGraph: Exploring Large-scale Graph Processing on Multi-FPGA Architecture*

Monterey, CA, USA Feb. 2016

- *FPGP: Graph Processing Framework on FPGA*

Visitings and Internships

Computing Platform-MaxCompute-Graph Compute, Alibaba Group Jul. 2018 – Oct. 2018

- Large-scale graph embedding/learning acceleration

Institute of Parallel and Distributed Systems, Shanghai Jiao Tong University Jul. 2017 – Aug. 2017

- Large-scale graph processing on distributed systems

IBM Research China Jul. 2013 – Aug. 2013

- Scheduling of heterogeneous cloud computing based on FPGA virtualization

Patents

"FPGA (field-programmable gate array) virtualized hardware architecture communication method and device"

- Inventor: **Guohao Dai** Yuliang Sun Dan Tian Yu Wang Publication Number: CN106776002A

Academia and Teaching Services

Reviewer of IEEE Transactions on Parallel and Distributed Systems Aug. 2018 – now
Reviewer of Journal of Circuits, Systems, and Computers Mar. 2018 – now
Teaching assistant in the course "Digital Logic Circuit and CPU Design" Mar. 2017 – Jun. 2017
Teaching assistant in the course "Digital Logic Circuit and CPU Design" Mar. 2016 – Jun. 2016
Teaching assistant in the course "Logical Design of Digital System" Sep. 2014 – Jan. 2015

Social Services

Counselor of undergraduate students Sep. 2014 – Jul. 2016

- *Advanced Class Collective Honorary*, Beijing Municipal Education Commission
- *Advanced Class Collective Honorary*, Tsinghua University

Vice chair of Student Union of E.E, Tsinghua Jun. 2013 – May. 2014

Skills and Languages

- **Programming language**: C/Unix programming, C++, Verilog, CUDA, Python, etc.
- **IDE**: Vivado/ISE, Quartus, Modelsim, Multisim, Visual Studio, Matlab, PyCharm, etc.
- **English level**: IELTS (7.0)