Haixiao Du

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Experience

09/2011 - present	**Tsinghua University** Ph.D. in Department of Electronic Engineering, Advisor: Prof. Huazhong Yang.
09/2007 – 07/2011	Beijing Institute of Technology B.S. in School of Information and Electronics
09/2004 – 07/2007	Beijing No. 4 High School

Research Summary

My research direction covers bioinformatics, high-performance/parallel computing, and computer aided design. My current and past research interests are:

- Hybrid CPU-GPU platform for fast analysis of voxel-wise MRI data analysis

  The platform aims at accelerating the frequently used but time-consuming algorithms provided by a combination of non-invasive neuroimaging techniques and graph theoretical approaches in the research of human connectome. The toolbox provides functions for the construction and the analysis of voxel-wise brain networks from resting-state fMRI data. The platform can reduce the run time of the whole analyzing process from days per subject to hours, even minutes.

  1 paper was published in [PLOS ONE 2013]. The source code is released on the website http://parabna.weebly.com.

- Clock tree synthesis (CTS) in 3D ICs

  Through-silicon via (TSV) could provide vertical connections between different dies and has been widely used in three-dimensional integrated circuits (3D ICs), but the silicon area occupied by TSVs may bring great challenge to designers in 3D clock tree synthesis. We focus on this practical issue caused by TSVs, which has been ignored in most previous works, and propose TSV-aware clock tree topology generation method and whitespace-aware TSV arrangement strategy in 3D clock tree synthesis.

  2 papers were published in [ISQED 2013] and [ISVLSI 2013].

Journal Publications

[PLOS ONE] Yu Wang , Haixiao Du, Mingrui Xia, Ling Ren, Mo Xu, Teng Xie, Gaolang Gong, Ningyi Xu, Huazhong Yang, Yong He. (2013) A Hybrid CPU-GPU Accelerated Framework for Fast Mapping of High-Resolution Human Brain

Connectome. PLoS ONE, 8(5): e62789,

Conference Publications

[ISQED] Wulong Liu, Haixiao Du, Yu Wang, Yuchun Ma, Yuan Xie, Jinguo Quan, Huazhong Yang: TSV-aware topology generation for 3D Clock Tree Synthesis. ISQED 2013: 300-307
[ISVLSI] Xin Li, Wulong Liu, Haixiao Du, Yu Wang, Yuchun Ma, Huazhong Yang: Whitespace-aware TSV arrangement in 3D clock tree synthesis. ISVLSI 2013: 115-120

Honors and Awards

2013	IBM Excellent Student Scholarship awarded by China Scholarship Council and IBM China
2012	TOP 10, AMD China Heterogeneous Development Contest 2012
2011	Excellent Undergraduate Award in Beijing Institute of Technology
2009	National Scholarship, awarded by Ministry of Education of China
2008	National Scholarship, awarded by Ministry of Education of China

Technical Skills

- General programming: C/C++
- GPU programming: CUDA
- MATLAB
- R Language